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THE WORLDWIDE TECHNOLOGY WEEKLY
OCTOBER 7, 1985

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LASER IS THE LATEST LIFE EXTENDER
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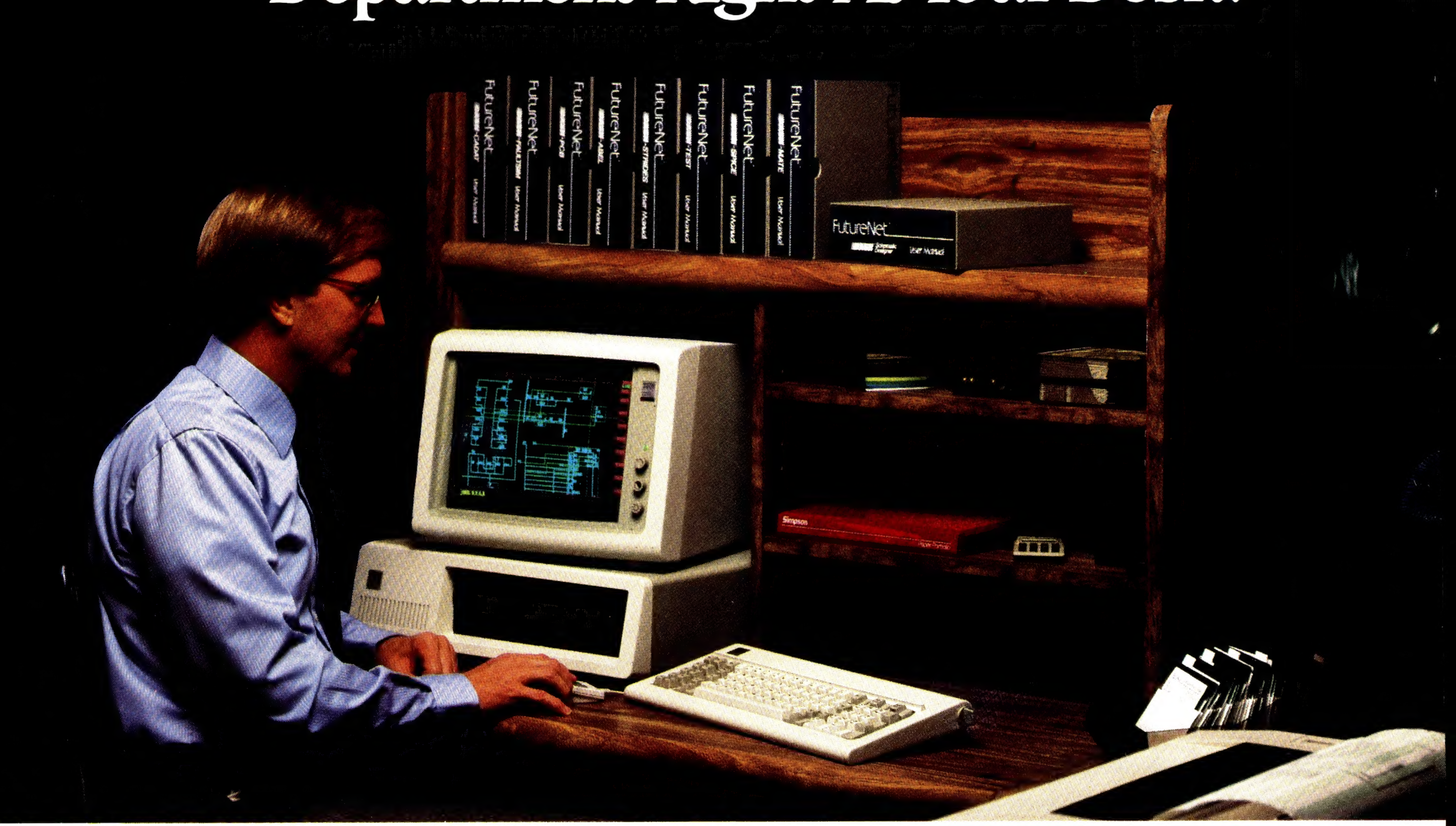

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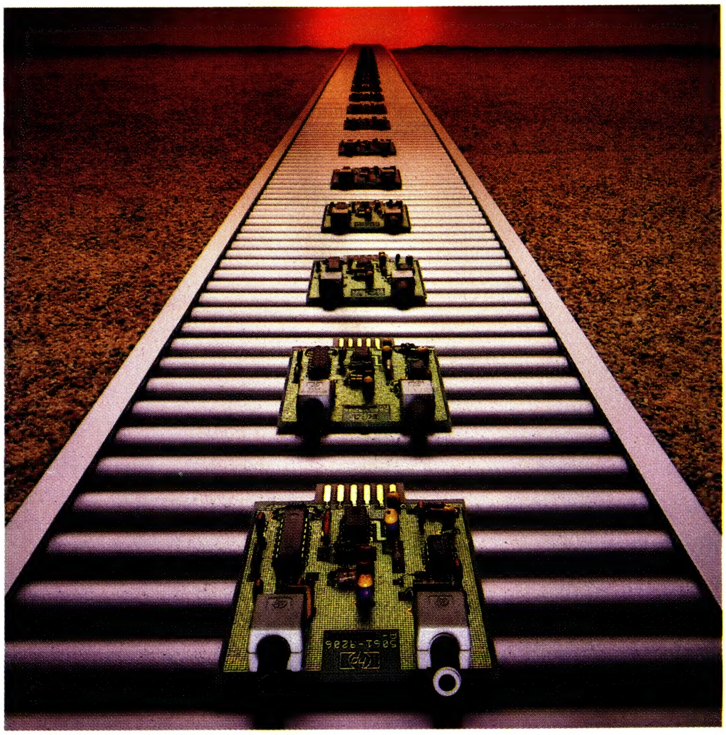
Low-cost fiber-optic components for high-volume manufacturing.



Lower manufacturing costs.

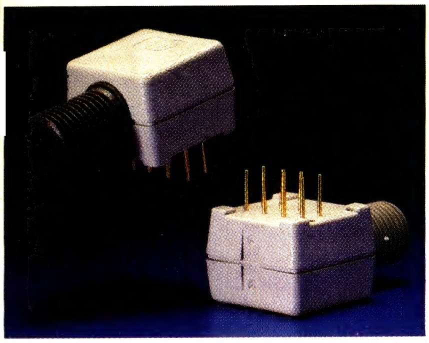
Finally you can reap all the benefits of using fiber-optic components for no more than the cost of using line drivers.

HP's new miniature fiber-optic components are housed in an integrated dual-in-line package designed for high-volume manufacturing—just like any other IC chips.

Auto-insertable and wave-solderable, the HFBR-0400 family of components is molded of high strength, heat-resistant and flame-retardant plastic. Mounting hardware and receptacles are eliminated, saving you money.

Design flexibility.

You have a choice of standard optical power or high-performance transmitters and of analog or digital receivers. You can achieve data rates up to 40 MBaud or analog bandwidths as high as 25 MHertz.



Each component is available for use with five fiber sizes—100/140, 50/125, 62.5/125, and 85/125 micrometre glass cables and 200 micrometre plastic-coated cable.

The optical port interfaces directly with standard SMA connectors.

Proven reliability.

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For pricing and delivery, contact your authorized Hewlett-Packard components distributor. In the U.S., call Hall-Mark, Hamilton/Avnet or Schweber. In Canada, call Hamilton/Avnet or Zentronics, Ltd.

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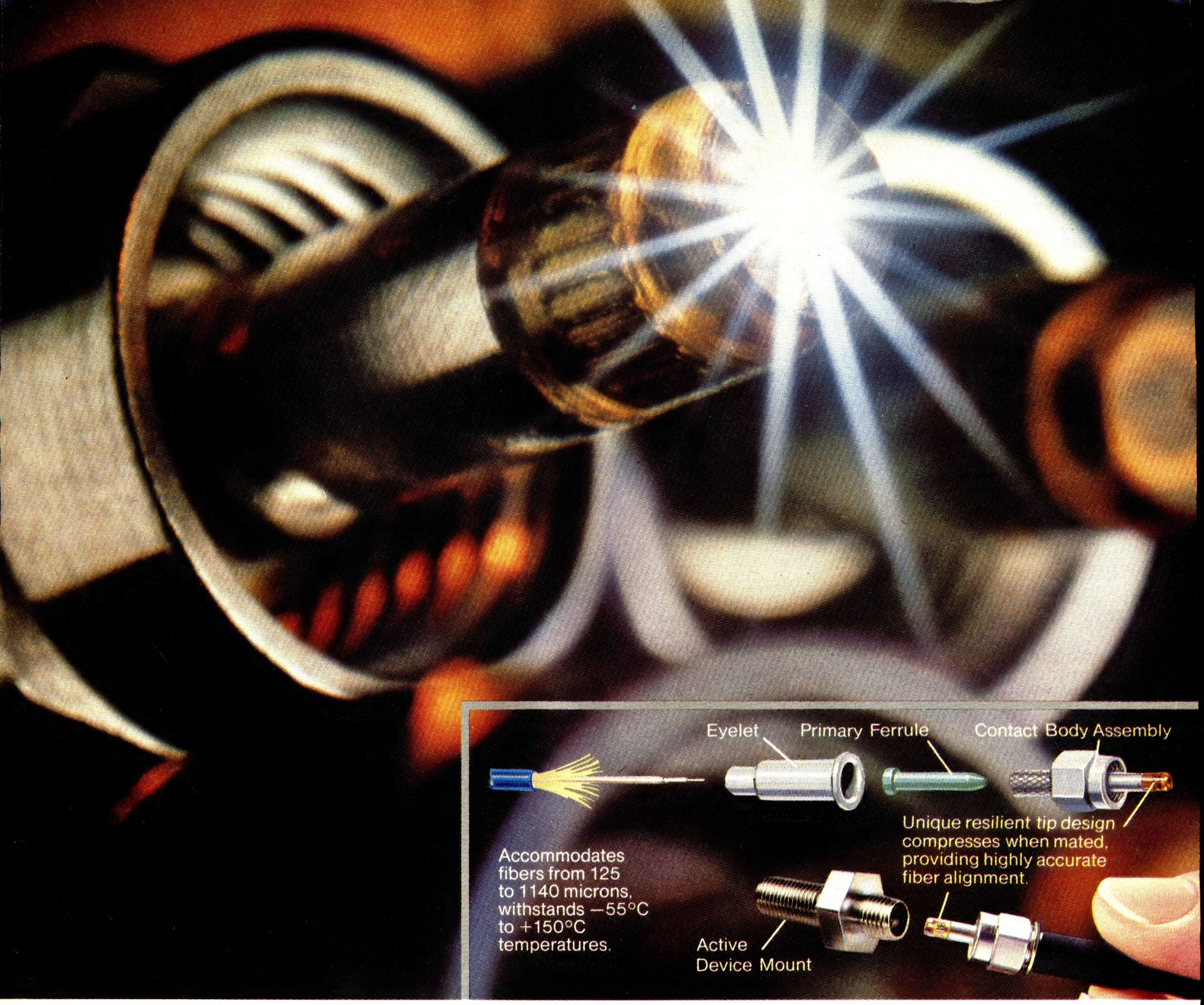
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Electronics

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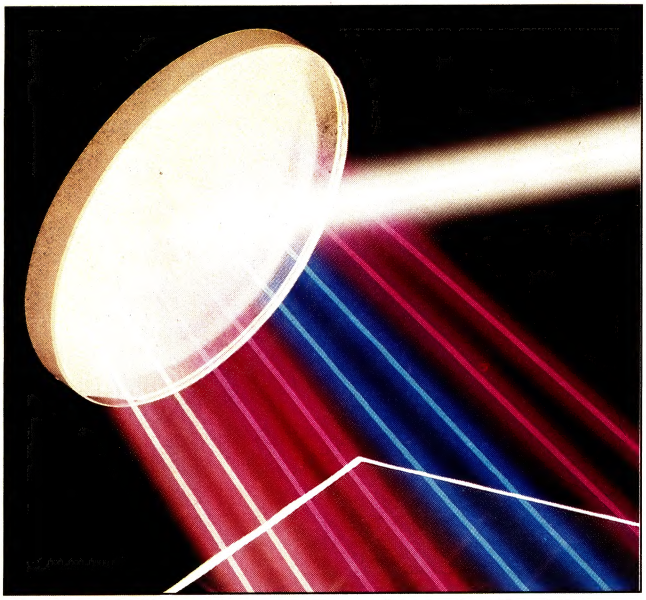

COVER: Optical lithography refuses to die, 36
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New tools will aid customer-designed arrays, 30
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PUBLISHER'S LETTER

What happens when a hurricane roars up the East Coast, forcing Manhattan's office towers to close? As far as the somewhat overestimated Hurricane Gloria is concerned, the result was not so much havoc wreaked on life and property but on magazine production schedules. Some people managed to rearrange their schedules by putting off tasks for a day, but others simply had to ignore rain and wind because their timetables leave no room for adjustments.

UNDETERRED. A hurricane doesn't faze Ciatto & Co.

One such group, which routinely manages to work through disasters both natural and man-made, is the *Electronics* editorial production department. Under the guidance of manager Charles D. Ciatto, June Noto and Jody LoGrasso routinely and calmly do their job of getting the words and illustrations produced in New York into page form and then to the facility in New Jersey, where they are made into film that eventually winds up at the printing presses in Virginia.

"If we go home, then the magazine doesn't get printed," says Charlie, who has ridden out many rain and snowstorms in his 16 years on the magazine. "That's why we can't let things like Hurricane Gloria get in the way. In fact, the worst thing that I imagine can ever happen to us is a power failure, and in that event we would just go to our emergency backup plan."

One of the crosses that the trio has to bear is that it is at the end of the editorial production line: every writer, editor, and artist has to complete his or her work before the editorial production people can start theirs. That is why on most nights one or more of Charlie's crew is still creating page specifications on the terminals of our Atex system long after everyone else has gone home.

"At least we have all this sophisticated high-tech equipment to help us do the job," says Charlie. "With our Atex computerized editorial-production system, we can do in minutes what used to mean an overnight job in the days of typewriters and hard copy. And that 'soft screen,' which enables us to display the page that we have built and check it for proper fit, saves countless hours each day."

But in the final analysis, what Charlie, June, and Jody have is a high degree of dedication to their mission.

This week we launch the second decade of our annual Technology Update. The first of the five-part series, written by our staff specialists, begins on p. 49 and covers computers. The others will follow each week and examine, in order, semiconductors, communications, manufacturing, and consumer electronics. The update will analyze the important trends in each segment.

Laurence Altman

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WEEK 1

Who says there's nothing good on the tube? There sure is now. Our new *Graphics Color Palette chip, the Am8151.*

It's a truly integrated, truly high performance IC that is going to foment a revolution in resolution. All by delivering the previously unobtainable: Extremely high resolution with a refresh rate high enough to completely eliminate flicker.

New CRT chip dazzles in triumphant screen debut.

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This is the first IC to combine a 256-byte color map, a low-glitch d-a converter, three pixel-data and two monitor-control pipeline registers, a voltage reference, and monitor control signals on a single chip.

Practical advantages are enormous. A palette approach that slashes overhead, making it easier to manipulate colors.

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WEEK 2

WEEK 3

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WEEK 4

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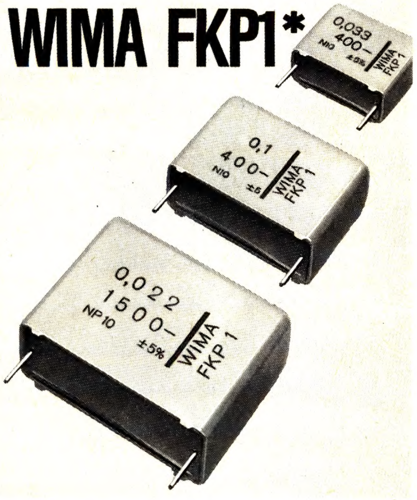

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MEETINGS

Cellular Communications '85, Online International Inc. (989 Avenue of Americas, New York, N. Y. 10018), New York Hilton, New York, Oct. 28-30.

12th Computer Security Conference and Exhibition, Computer Security Institute (43 Boston Post Rd., Northborough, Mass. 01532), Hyatt Regency O'Hare, Chicago, Nov. 4-6.

International Electronic Components Exhibition, French Federation of Electrical and Electronics Industries (SDSA, 20 rue Hamelin, 75116 Paris, France), North Paris Exhibition Grounds, Paris, Nov. 4-8.

Gomac-85: Government Microcircuit Applications Conference, Department of Defense *et al.* (Palisades Institute for Research Services Inc., 201 Varick St., Suite 1140, New York, N. Y. 10014), Marriott Hotel, Orlando, Fla., Nov. 5-7.

ISHM '85: International Symposium on Microelectronics, International Society for Hybrid Microelectronics (P. O. Box 3255, Montgomery, Ala. 36109), Disneyland Hotel, Anaheim, Calif., Nov. 11-14.

1985 GaAs IC Symposium, IEEE (James A. Hutchby, Technical Program Chairman, Research Triangle Institute, P. O. Box 12194, Research Triangle Park, N. C. 27709), Monterey Conference Center, Monterey, Calif., Nov. 12-14.

International Conference on Systems, Man, and Cybernetics 1985, IEEE (Russ Ferrell, Systems and Industrial Engineering Department, University of Arizona, Tucson, Ariz. 85721), Holiday Inn-Broadway, Tucson, Nov. 12-15.

Fiber Optics: Trends and Directions '85, Electronic Industries Association (2001 Eye St. N. W., Washington, D. C. 20006), Silverado Hotel, Napa, Calif., Nov. 18-20.

Iecon '85: 11th IEEE Industrial Electronics Society Conference, IEEE (Ravi Prakash, Thomas J. Watson Research Center, Mail Stop 3-249, P. O. Box 218, Yorktown Heights, N. Y. 10598), Hyatt Regency, San Francisco, Nov. 18-22.

CIPS Conference, Canadian Information Processing Society (243 College St., Toronto, Ontario, M5T 2Y1), International Centre, Toronto, Nov. 18-22.

SCAE 1985, Society for Computer-Aided Engineering and American Fabricating Institute of Technology (Jan Dolman, Exposition Coordinator, American Fabricating Institute of Technology, 7811 N. Alpine Rd., Rockford, Ill. 61111), Astro Village Hotel Exhibition Center, Houston, Nov. 19-20.

ITC '85: International Test Conference, IEEE (ITC '85, P. O. Box 264, Mount Freedom, N. J. 07970), Marriott and Adam's Mark hotels, Philadelphia, Nov. 19-21.

Circuit Expo '85, Worldwide Convention Management Company (17730 W. Peterson Rd., Libertyville, Ill. 60048-9989), Sheraton, Boston, Nov. 19-21.

Wescon '85, IEEE (Electronics Conventions Management Inc., 8110 Airport Blvd., Los Angeles, Calif. 90045), Moscone Convention Center, San Francisco, Nov. 19-22.

Conference on Factory Automation Models and Standards, National Bureau of Standards and U. S. Navy (U. S. Department of Commerce, National Bureau of Standards, Gaithersburg, Md. 20899), NBS Facility, Gaithersburg, Nov. 20-21.

Canadian Programmable Control Conference and Exhibition, IEEE (Kerrwil Publications Ltd., Trade Show Division, 501 Oakdale Rd., Downsview, Ontario, Canada M3N 1W7), Hamilton Convention Centre, Hamilton, Canada, Nov. 20-21.

Comdex/Fall '85, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Convention Center *et al.*, Las Vegas, Nev., Nov. 20-24.

Scan-Tech Europe '85, Automatic Identification Manufacturers Inc. (AIM, 1326 Freeport Rd., Pittsburgh, Pa. 15238), Jaarbeurs Congress & Exhibition Centre, Urtrecht, the Netherlands, Nov. 25-28.

Infocoms, RAI Gebouw BV and Industrial Presentations (Europe) BV (Amsterdam RAI, Europaplein, Amsterdam, Holland), RAI Exhibition Centre, Amsterdam, Nov. 26-29.

International Test and Measurement Exhibition and Conference '85, Network Events Ltd. (Printers Mews, Market Hill, Buckingham, MK18 1JX, England), Olympia 2, London, Nov. 27-29.

IEDM: 31st International Electron Devices Meeting, IEEE (Electron Devices Society of the IEEE, 655 15th St. N. W., Suite 300, Washington, D. C. 20005), Washington Hilton and Towers Hotel, Washington, Dec. 1-4.

Globecom '85: IEEE Global Telecommunications Conference, IEEE (G. A. Ledbetter, South Central Bell, 365 Canal St., New Orleans, La. 70140) Hyatt Regency, New Orleans, Dec. 2-5.

1st International Conference on Supercomputing Systems, IEEE (Supercomputing Conference, P. O. Box 639, Silver Spring, Md. 20901), Innisbrook Resort, Tarpon Springs, Fla., Dec. 16-20.

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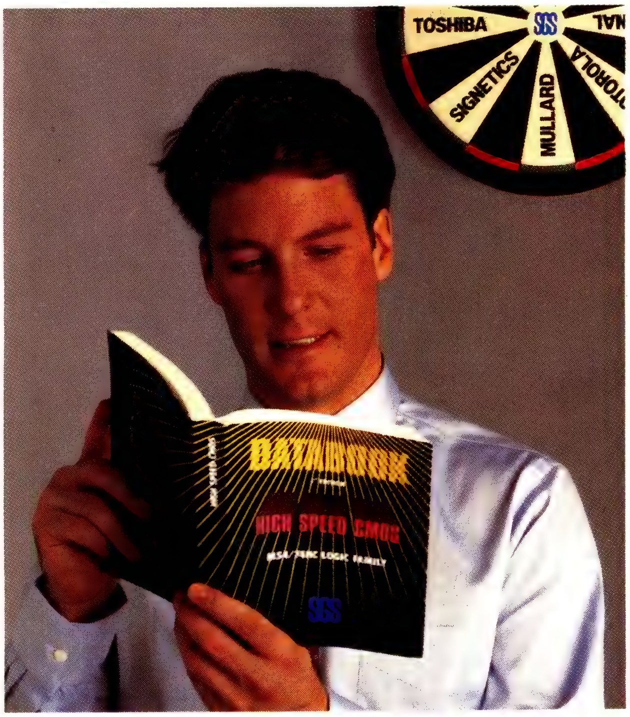

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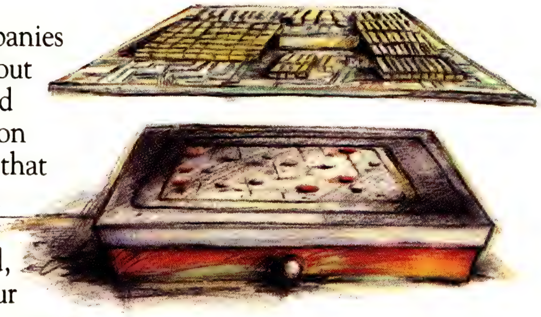

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ELECTRONICS NEWSLETTER

MOLECULAR-BEAM EPITAXY COMES TO GaAs

Molecular-beam epitaxy, with its more precise implantation of dopants, may soon appear in the production of gallium arsenide digital chips, thanks to a manufacturing system developed by Hitachi Ltd. that features automated wafer handling and an improved vacuum process. The new system, which puts epitaxial films on compound semiconductor wafers, is equally suitable for manufacturing high-electron- mobility transistors and lasers. The Tokyo company will put the system on the Japanese market by the end of next year for $700,000 to $930,000. Export sales will follow. Systems now available from other manufacturers have been designed for research rather than production, says Hideaki Kamohara, chief researcher at Hitachi's Mechanical Engineering Research Laboratory, where the system was developed. To develop automated operation, Hitachi had to come up with motors, air cylinders, and sensors that could withstand the bakeout temperature. □

TI MUM ON NEW VOICE-VERIFICATION TECHNOLOGY

Texas Instruments Inc. is keeping a tight lip on a new voice-verification algorithm developed for its TMS32010-based speech-processing board. The signal-processing board slips into TI and IBM-compatible personal computers. The new algorithm is aimed at verification for security applications, says Roy Pursley, technology marketing manager for TI's Data Systems Group in Austin, Texas. Unlike TI's existing speech-recognition products, the voice-template matching software is not based on linear predictive coding. The add-on board—not including application software—retails for $995 and operates under Microsoft Corp.'s MS-DOS operating system. Attempts to systematically fool the program would succeed only four times in 10,000 tries. "It is very new. . . . We are not, at this point, ready to tell the world what the base technology is," says Pursley, who is considering partners to develop applications around the speech software. The first voice-verification application was disclosed by Voxtron Systems Inc., New Braunfels, Texas, during a recent corporate-security conference in Dallas. □

KOREA'S HYUNDAI CLOSES DOWN SANTA CLARA CHIP PLANT

The big Korean drive to penetrate the semiconductor marketplace is taking a backward step. Hyundai Ltd., the Seoul giant, closed its Santa Clara, Calif., semiconductor-fabrication plant, Hyundai Electronics America, that it opened just last year. Citing "continuing adverse market conditions," Hyundai laid off all 100 production employees. The future of about 100 other sales, marketing, administrative, and engineering employees is uncertain. Last October, Hyundai Group chairman Ju-Yung Chung touted the plant as "the beginning of a larger, more comprehensive high-technology role for Hyundai." The facility, which cost about $40 million to build, has lost at least $21 million so far this year. □

USE OF ADA FOR ALL NEW MILITARY AVIONICS GETS CLOSER

The Pentagon is a step closer to using the Ada programming language for all applications software in new avionics systems now that Westinghouse Electric Corp.'s Advanced Technology Division in Baltimore has successfully compiled and run an Ada program on its 1750A controller breadboard for Very High-Speed Integrated Circuits. The division has sent copies of its compiler to the Ada Validation Facility of the Federal Software Testing Center to begin the validation process. The controller consists of 16 VHSIC 64-K static random-access memories, developed during Phase 1 of the program, and an embedded controller now being populated with VHSIC circuits. □

ELECTRONICS NEWSLETTER

JAPANESE GET CLOSER TO CHIP REPLACEMENT FOR HELIUM NEON GAS LASER

Japanese researchers are getting close to grabbing the brass ring in semiconductor lasers: generating visible light at the 633-nm wavelength of helium neon lasers. This would eliminate the need to use the power-consuming gas lasers and their larger power supplies. NEC, Sony, and Toshiba are all working hard to develop solid-state versions. A semiconductor laser developed by Toshiba Corp. researchers operating at room temperature generates 679-nm continuous-wave oscillations with a power output exceeding 20 mW. NEC Corp. labs achieved cw oscillation at 689.7 nm with an output of about 1 to 2 mW, while Sony Corp. achieved cw oscillation at 672.1 mW with about the same output. All three lasers are double-heterojunction types with a thin active layer of indium gallium phosphide sandwiched between layers of indium gallium aluminum phosphide. All three were fabricated by metal organic chemical-vapor-deposition technology. But products won't come until researchers can produce tighter beams and ensure reliability. Sony appears to have the furthest to go: Toshiba and NEC lasers will oscillate at temperatures above 50°C; the limit for the Sony laser is 33°C. NEC is also developing a different solid-state laser [*ElectronicsWeek*, April 8, 1985, p. 23] that is made with a vapor-phase epitaxy process. ☐

LAYOFFS, CUTS CONTINUE DESPITE PREDICTION OF UPTURN

Look for layoffs and payroll trimming to continue in the slumping computer and semiconductor industries despite predictions by the Semiconductor Industry Association of an upturn in the fourth quarter. Intel Corp. said it will cut wages of all 14,500 U. S. workers by 4% to 8% and close all U. S. operations for six days at Christmas. The Santa Clara, Calif., chip maker has already cut its U. S. work force by over 1,800 this year, but says it is taking the action to avoid further layoffs. Another major chip maker, Motorola Inc., will cut worldwide employment in its Semiconductor Products Sector by about 1,700 workers in coming weeks. Half of the layoffs will occur in the U. S. Although last week's announcement marks the largest single cut to date for Motorola, it has trimmed its work force by a total of about 8,000 since last October. The company also said that employees will take pay cuts of 5% to 10% until March 31, 1986. Makers of peripheral equipment continue to feel the effect of the slump as well. Magnetic Peripherals Inc. announced it will close its Santa Clara disk-drive manufacturing plant by July 1986, eliminating 1,100 jobs in stages. ☐

APPLE PRICE CUTS MAY HERALD ANOTHER COMPETITIVE HOLIDAY SEASON

Personal computer makers are hoping the Christmas selling season will boost their sales in the same strong way the holiday period did last year. But to get sales moving skyward in 1984 took price cutting and deals, and industry observers expect to see the same thing happen again this year. Apple Computer Inc. didn't disappoint them. Last week it fired the initial salvo, dropping the price of the low-end Apple IIc to $995—21% less than the previous price of $1,295. Price tags on the Apple IIe and Macintosh were also cut by 17.5% and 10.5%, respectively. If IBM Corp. follows with lower prices on its Personal Computers, the move would be neither a comfort nor a joy to such troubled personal computer makers as Atari Inc. and Commodore Business Machines Inc. Atari is having a difficult time getting its $795 520ST off the ground, and Commodore, with an aging user base of Commodore 64 users, is trying both to sell an upgrade to the 64—the Commodore 128—and launch its new Amiga computer, which fully equipped costs more than $1,500. To launch the Amiga, Commodore claims it will spend more than $40 million on advertising and marketing. ☐

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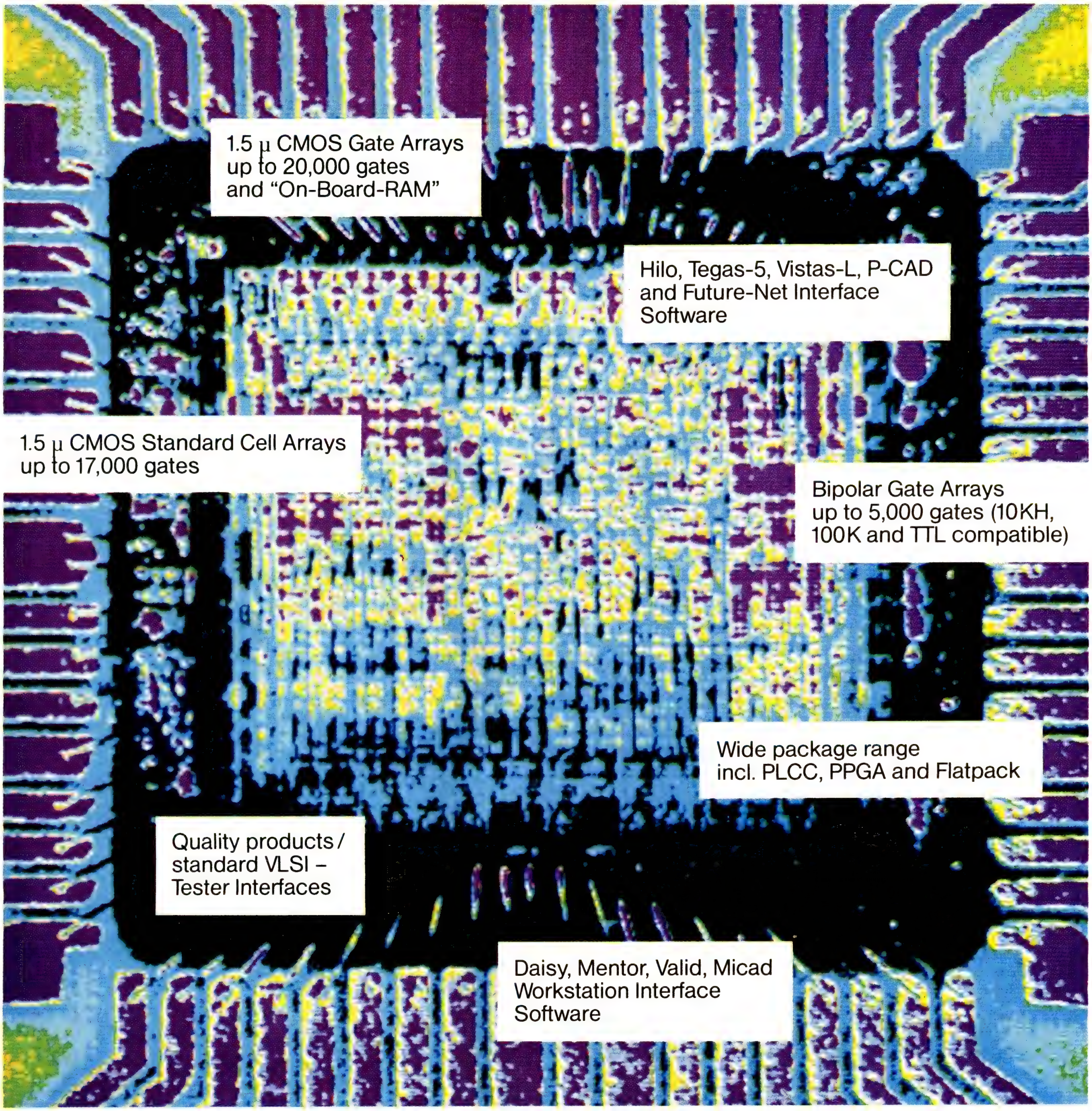

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Electronics

SILICON VALLEY TRIO PRESSES FOR DUMPING TAX ON EPROMS

AMD, INTEL, AND NATIONAL CALL JAPANESE PRICING PREDATORY

SANTA CLARA, CALIF.

For the fourth time in as many months, the U. S. chip-making industry—losing millions of dollars a month in its worst year ever—has pleaded for U. S. government help to withstand the onslaught of Japanese competition.

Three top U. S. chip makers petitioned the International Trade Commission last week for a dumping tax on Japanese erasable programmable read-only memories, contending their pricing was predatory. With their complaint that Japanese companies were illegally selling EPROMs below cost, the three Silicon Valley firms—Intel, National Semiconductor, and Advanced Micro Devices—followed up an initial call for help in June from the Semiconductor Industry Association. At that time, the SIA, filing under Section 301 of the Trade Act of 1974, asked the U. S. government to help in opening up Japanese markets [*Electronics,* June 17, 1985, p. 13]. The SIA warned then that Japanese firms were suspected of dumping.

The Justice Department has already begun an investigation of Hitachi Ltd., one of the eight companies named in the complaint, on charges of dumping EPROMs [*Electronics,* Aug. 12, 1985, p. 12]. In the meantime, Micron Technology Inc., of Boise, Idaho, has filed a separate dumping complaint against seven Japanese companies over dynamic random-access memories [*Electronics,* Aug. 5, 1985, p. 16] and coupled it with a civil antitrust claim for $100 million in damages.

Though he declined official comment because the latest action is against individual companies and not against the Japanese industry as a whole, Mamoru Tsukamoto of the Japan Electronics Bureau, in New York, unofficially described the continuing series of actions as "legal harassment."

R. Michael Gadbaw, a Washington attorney for the SIA, puts it differently. He says that the dumping case "is a part of that larger mosaic." Indeed, the existing complaints and lawsuits may be only half the battle, since the latest action in the escalating U. S.-Japan semiconductor wars comes as protectionist pressure is building in Congress.

But some think rock-bottom prices come from high yields

To back up the claim that Japanese EPROM prices are actually below cost and therefore dutiable under an amendment to the Tariff Act of 1930, the trio of companies point to an analysis of Japanese production costs that was prepared by Washington economist William A. Finan.

Operating with data supplied primarily by Intel, Finan estimates that quoted Japanese prices were below "fair value"—including an 8% profit mandated by the trade law—by $2.22 for 64-K, $3.28 for 128-K, and $2.97 for 256-K EPROMs. These are the amounts the petitioners want tacked on as duties.

Otherwise, they warn, U. S. firms will lose more than $200 million in revenue in the next year and may be squeezed out of the market altogether. "The Japanese industry's strategy of steadily gaining market share by . . . selling at prices apparently unrelated to cost was successful in the case of the 64-K DRAM, where the Japanese currently account for 70% of the market and U. S. producers are operating at a loss or have left the market entirely," the petition says. "The Japanese strategy will be equally devastating in the U. S. EPROM market, unless antidumping duties are imposed."

GOING PUBLIC. The dumping charges were made public at a news conference run by Intel corporate attorney F. Thomas Dunlap Jr., who displayed charts showing precipitous price declines in EPROMs of all densities since January. Until June, U. S. quotes lagged a month or so behind the Japanese, according to Dunlap's demonstration. Since then, the two industries have slugged it out toe to toe.

Not all industry analysts agree that the Japanese companies were selling below cost; some suspect that greater yields might have allowed them to cut prices sharply. One observer faults Finan's estimate that Hitachi, which is considered the most efficient Japanese producer as well as the largest, had wafer-sort yields of 40% on 64-K, 30% on 128-K, and 21% on 256-K EPROMs. These estimates are much too low, perhaps by as much as half, in the view of William J. McClean of the Integrated Circuit En-

POINT MAN. Intel counsel F. Thomas Dunlap Jr. produced numbers that show how U. S. prices for EPROMs of all types have dropped precipitously since January in the U. S. market.

gineering Corp., Scottsdale, Ariz.

McClean also challenges as too large the 205-by-205-mil die size Finan attributes to the Hitachi 64-K EPROM. Comparable chips have half the area, he indicates, which would provide more candidate dice per wafer and greater yields from a given number of defects.

Finan's analysis does not list calculated defect density. But McClean says most Japanese companies were operating at three defects per square centimeter or better, which would predict greater yields than the Finan model.

"I don't believe that the Japanese are selling below manufacturing cost," McClean says.

In general, the Japanese have kept a low profile in replying to the charges. A short Hitachi statement called them "without foundation." And one source within Hitachi said privately that the company had less than 3% of the U. S. EPROM market and did not have the lowest prices.

Texas Instruments Inc., in Dallas, which recently unveiled a high-voltage CMOS technology for its new push in EPROMs [*Electronics*, Sept. 30, 1985, p. 16], issued a carefully worded statement supporting "vigorous enforcement" of anti-dumping laws but declining to join in the petition. TI is itself a major IC producer in Japan, where it has three semiconductor plants.

The dumping petition will begin its trek through the trade-regulation process with an International Trade Commission hearing within 21 days. Final determination of the case should come next year—as early as July or as late as October. *–Clifford Barney*

SEMICONDUCTORS

TOSHIBA SET TO ENTER POWER MOS FET MARKET

LOS ANGELES

Efforts by U. S. semiconductor vendors to get government help in protecting domestic markets has not scared off Toshiba Corp. from taking aim at one of the fastest-growing semiconductor sectors—power MOS FETs. Toshiba expects to have four new products ready before year end to propel itself into the booming sector.

The timing surprised many marketing officials at U. S. MOS FET companies. They had expected all along that heavyweight Japanese competitors would be lured by the heady growth of the market. But the consensus pegged the first arrival as months, if not years, away [*Electronics*, June 17, 1985, p. 24]. Also coming as somewhat of a surprise is that Toshiba leads the way at this point rather than Hitachi Ltd., which U. S. companies identify as the leading domestic Japanese MOS FET supplier.

LEAPFROG STRATEGY. But the limited device specifications that Toshiba has made available so far reveal a well-reasoned strategy. The Kawasaki company is opting to leapfrog—for now at least—the lower-range power MOS FET arena (current ratings from 1 to 10 A at 100 to 500 V) where U. S. producers battle it out, turning out millions of chips per month. Instead, Toshiba will address the higher levels (25 to 50 A at 500 to 1,000 V). At this level, MOS-type structures in power devices do not yet claim a comparable foothold against less expensive established bipolar chips, Darlington transistors, or hybrid modules. Thus far, no company has carved out a dominant position in this range.

Toshiba claims it is not targeting the U. S. in particular. "We want to sell where we can. We've marketed these products worldwide," says a Toshiba spokesman. Since announcing its first MOS FET last October, Toshiba's sales already have amounted to $5.6 million worldwide, primarily in Japan. This rates as a fast start for any product, especially during a recession. "This is very smart on Toshiba's part," comments industry consultant Will Strauss, founder of Forward Concepts Inc., Scottsdale, Ariz.

Toshiba plans to leapfrog the low-power arena

Strauss, for one, is not among those surprised by the Toshiba move. He calls them "the most aggressive company in the discrete [component] business." A year ago, Toshiba ranked third among worldwide discrete suppliers, he points out, but it already has pulled ahead of Tokyo's NEC Corp.

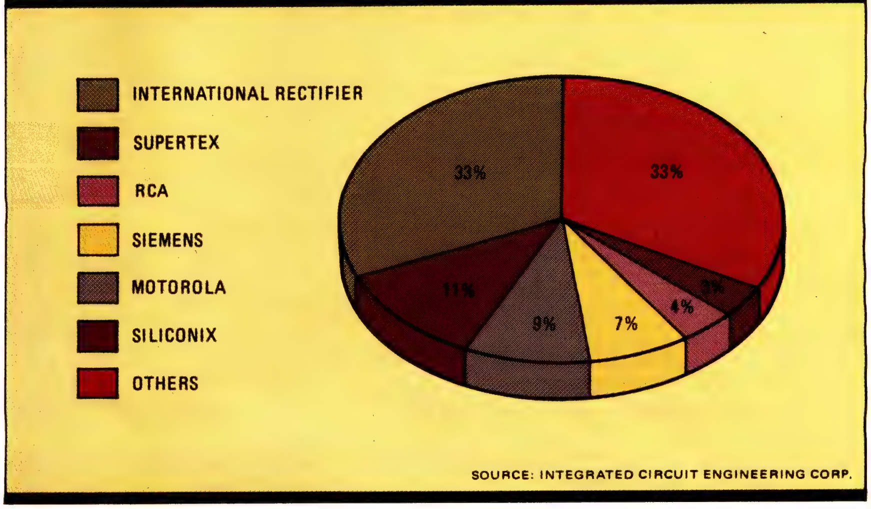
With high-power MOS FETs initially aimed at controls for motors of 1 hp and up, Toshiba is tackling a business in which it has roots at home and elsewhere, notes Derek Lidow, executive vice president at International Rectifier Corp., El Segundo, Calif. "They and Mitsubishi own that market."

FAST GROWTH. Lidow's company led MOS FET suppliers last year (see chart) and still maintains the largest market share worldwide, according to most estimates. International Rectifier's lower-power chips go into fractional-horsepower motor controls for such applications as disk drives and computer peripherals, along with industrial power uses.

More high-power MOS applications could open up fast, says Erik Jansen, marketing manager for power MOS products at Siliconix Inc., Santa Clara, Calif. "There definitely is an awful lot of business, as a natural evolution going to higher current and higher voltages," he observes. Toshiba views applications in robotics and precision control equipment as most promising. Siliconix intends to contend strongly for higher power growth and will open a new 6-in.-wafer fabrication line later this year to turn out improved products.

Although neither Toshiba nor any other Japanese producer is yet going after the entire spectrum of MOS FET customers in the U. S., the time will come soon, most observers agree. Market growth alone ensures that—to nearly $700 million by 1990, according to recent projections by Integrated Circuit Engineering Corp., Scottsdale. (ICE market estimates are based on dollars received by the manufacturer without taking into ac-

INTERNATIONAL RECTIFIER LEADS IN POWER FETS WORLDWIDE



SOURCE: INTEGRATED CIRCUIT ENGINEERING CORP.

count markups from distribution or other sales channels.)

Another factor supporting expansion of Japanese suppliers to the U. S. stems from the consumption rate of discrete components, where the U. S. until recently led Japan, points out ICE market-research analyst Dean A. Winkelmann. But during the first half of 1985, the Japanese for the first time surpassed the U. S. in consumption of discretes, using some $902 million worth to build equipment compared with about $766 million in the U. S.

The future implications are clear to Winkelmann, both for MOS FETs and other components. "All the integrated Japanese firms have to do is open their captive doors and let the products flow out." *–Larry Waller*

HAS THE AGE OF VLSI ARRIVED FOR GaAs?

RYE BROOK, N. Y.

So far, gallium arsenide integrated circuits have touched off excitement mostly among people involved in solid-state device development. But at this week's International Conference on Computer Design (ICCD) in Rye Brook, the excitement should ripple through computer designers as well: a total of seven papers and one panel are devoted to GaAs very large-scale-integration technology.

The excitement has built to the point where Purdue University researcher Veljko Milutinovic proclaims that the age of VLSI has arrived for GaAs. Actually, the circuit densities that most researchers in GaAs are now getting for logic circuits and memories are just approaching LSI. But they are becoming technically and economically feasible for computer designs.

"There have been several significant advances [in digital GaAs chips] worldwide in the past year," says Joe Mogab, director of materials and wafer processing at Microwave Semiconductor Corp., the Siemens AG subsidiary in Somerset, N. J. He notes, for example, that Nippon Telegraph & Telephone Corp. has demonstrated a 16-K static random-access memory containing over 100,000 FETs.

Milutinovic will describe an 8-bit GaAs microprocessor that was developed jointly by Purdue and RCA Corp. The team also has a 32-bit chip in the works.

GIANT ARRAY. Another good example of the levels GaAs is reaching will come from Hitachi Ltd. Hitachi researchers will talk about logic-circuit technology for a 1,600-gate array based on GaAs enhancement/depletion-mode switches with buffered FET logic. At other sessions, the state of the art of a full range of GaAs technologies will be aired, says Mogab, who is chairing a full day of papers on GaAs.

Not all that's noteworthy in GaAs will be in evidence at Rye Brook. In Japan, the major computer companies—NEC, Toshiba, Mitsubishi, and Hitachi—are working with GaAs, in addition to telecommunications giant NTT.

Although Toshiba Corp. does not make mainframe computers, it sees a need for GaAs circuits in high-speed minicomputers. A Toshiba researcher says that device-integration levels in his lab are 4-K for SRAMs and 2,000 gates for arrays. Practical integration levels with present technology are 1-K for SRAMs and 500 to 2,000 gates for arrays.

These levels depend on configuration and packaging. With forced-air cooling, heat dissipation could be 3 to 4 W per chip—sufficient for a chip with 3,000 to 5,000 gates. With liquid cooling, dissipation could go to 10 W for 8,000- to 10,000-gate chips.

In its labs, Hitachi has achieved a 4-K SRAM as well as the 1,600-gate array. Hitachi researchers believe that in 1988, 4-K SRAMs should be ready for computers. It will probably take five years to get to VLSI levels, they say.

A NEC spokesman says that the company's GaAs research group has developed 1,000-gate logic devices and 4-K SRAMs. The R&D group believes GaAs will first be used in computers in the form of logic circuits with several hundred gates and cache memories. Attainable integration levels now are 3,000-gate logic circuits and 4-K SRAMs, they say. Future realizable integration levels are logic circuits with more than 10,000 gates and 256-K SRAMs.

To climb to higher levels of GaAs integration, researchers at Toshiba, Hitachi, and NEC say, complementary logic will be needed to decrease power dissipation. Other crucial areas include fine-pattern lithography, improved isolation, high-quality epitaxy, and larger, better-quality wafers. As for Fujitsu, a researcher there maintains that defect-free 3-in. wafers are the most important need for building VLSI.

–Tom Manuel and Charles L. Cohen

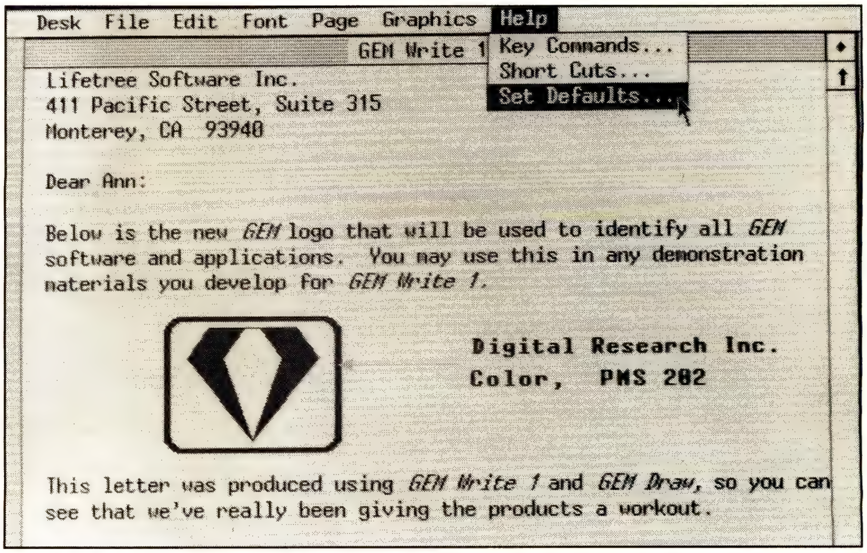
SOFTWARE

APPLE SHUTS WINDOW ON LOOK-ALIKE ICONS

PALO ALTO

Software developers may have to start paying closer attention to the way they design graphics interfaces—those mouse-driven icons, windows, and pull-down menus that are becoming popular design features for ease of use in personal computer software. If they look too much like someone else's, a lawsuit claiming violation of "visual copyright" could be in the making.

The latest victim of this concept—termed "nebulous" by some lawyers—is Digital Research Inc., a developer of



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411 Pacific Street, Suite 315
Monterey, CA 93940

Dear Ann:

Below is the new *GEM* logo that will be used to identify all *GEM* software and applications. You may use this in any demonstration materials you develop for *GEM Write 1*.

Digital Research Inc.
Color, PMS 282

This letter was produced using *GEM Write 1* and *GEM Draw*, so you can see that we've really been giving the products a workout.

LOOK-ALIKES? DRI will rework its GEM graphics environment manager (above) so that icons and windows on its screens won't resemble those of Apple's Macintosh (right).

software for personal computers. Last week, the Pacific Grove, Calif., company signed an agreement with Apple Computer Inc., Cupertino, Calif., to "substantially differentiate" certain applications programs in its Graphics Environment Manager (GEM) product line from those programs running on Apple's Macintosh. To stave off litigation, DRI also agreed to pay Apple an undisclosed amount in damages.

Apple says the interface of GEM, the operating system for the Atari 520ST and the British Apricot personal computer, uses icons, windows, and pull-down menus in a way "substantially similar" to the Mac's, though the Mac interface was not developed by Apple. It was the work of computer scientist Alan Kay at Xerox Corp.'s Palo Alto Research Center.

Can a picture of a garbage can be copyrighted?

Many computers, including Xerox's Star, and Sun Microsystems Inc.'s work stations, use the black-on-white screen with icons that resemble the Macintosh's. But Apple was undeterred from pursuing DRI.

"This is not a discussion of technology," says Apple's Kathleen Dixon of the Xerox PARC design. "Alan Kay's design looked different than ours."

Apple claims the precedent for its action was set around 1980 in the video-game business. Atari Inc. and Bally Midway Manufacturing Co., an arcade-game company that utilized Atari games, sued Magnavox for selling a cartridge game called KC Munchkin, which the courts found under copyright law to be a knockoff of Atari's best-selling PacMan arcade game.

Gordon Davidson, an attorney who has worked with Apple on previous copyright cases, says the courts then established a test he refers to as the "Standing 10 Feet Away and Squinting Test"—does it look the same from 10 feet away? "In this case," he says, "the court viewed the games and, despite their differences, said the visual impressions were substantially similar."

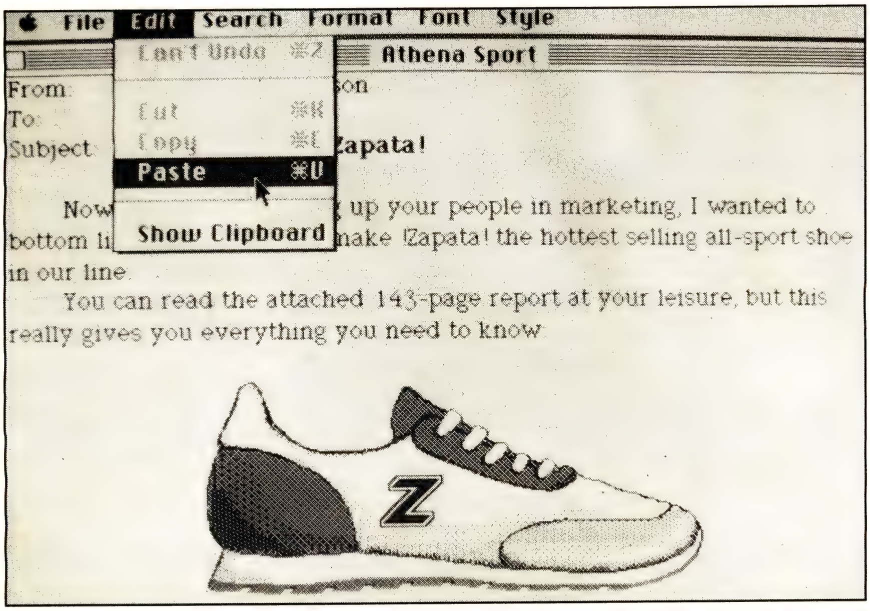
Dixon says the question is a matter of degree: exactly how much one product looks and acts like another. Apple claims that some parts of the GEM Desktop operating environment, as well as some GEM applications programs such as GEM Paint and GEM Draw, are nearly identical to the programs with the same function on the Macintosh. For example, both include such icons as a trash can symbol for deleting files.

Other companies such as Microsoft Corp. have released applications software that looks very similar to Apple's programs. Though a Microsoft spokesman said the company wasn't concerned with a lawsuit, Apple claims to be examining Microsoft products.

Apple says video games and applications software are the same under visual copyright laws. But one industry watcher finds this philosophy hard to swallow. "All the technology [including the look of the interface] came from Xerox," says Jan Lewis, president of the Palo Alto Research Group. "Can you really copyright a picture of a garbage can? . . . I find it a little bizarre that they can enforce copyright on such things."

Judy Mervis of DRI says the rework of GEM must be finished by Nov. 15, but involves only cosmetic changes.

Tom Byers, former product manager for GEM, says the agreement "sounds like someone [at DRI] has made a business decision." Apple claims DRI has agreed to work with it on future software projects. *–Denise Caruso*



From: son
To:
Subject: Zapata!

Now up your people in marketing, I wanted to bottom li make Zapata! the hottest selling all-sport shoe in our line.

You can read the attached 143-page report at your leisure, but this really gives you everything you need to know.

COMPUTERS

IBM GOES AFTER NUMBER CRUNCHING

RYE BROOK, N. Y.

In what many called the worst-kept secret in the computer industry, IBM Corp. last week brought out a vector-processing extension for its new Sierra 3090 mainframes. IBM says the internally installed hardware—which performs numerical calculations on whole arrays with single instructions—increases a 3090's speed from one and a half to three times when running engineering and scientific programs, yet it only increases processor floor space by 20%.

Though the market for this type of processing power is small and the revenue payoff will not be immediate, offering vector processing is an important strategy for IBM, market analysts point out. With the new vector-processing hardware, IBM is positioning itself more strongly in the scientific and engineering communities as it seeks new growth areas to sustain its future revenue growth. IBM last week also pushed up the delivery date for its largest new mainframe product, the 3090 model 400.

"The scientific community is not geared to IBM mainframes as number crunchers," says Matt Meehan, who follows IBM for Salomon Brothers Inc., a New York investment banking house. "But a lot of these people work for places that have IBM mainframes."

Meehan says his company surveyed users of computer equipment for scientific applications and found that 90% of them received their data from IBM mainframes and then manipulated that data on computers made by other vendors, such as Control Data Corp. Of this 90%, "a substantial number indicated that they would be very interested in this type of [vector-processing] machine from IBM," he continues.

A GOOD DEAL. "It looks like a really good deal for mainframe users with a lot of modeling or computational needs," says Carol E. Muratore, an IBM watcher with Prudential-Bache Securities Inc., New York. "It's a nice performance increase for a minimal amount of money."

Still, this market is not a huge one by the standards of IBM, which had revenue of almost $46 billion in 1984. IBM estimates that roughly 10% of all users of its 308X mainframe family are in the scientific community, and that about half of those users would be interested in the new vector facility. This would yield only a few hundred million dollars a year in revenue for IBM. The new vector product is available only on the 3090 family, IBM said. It will have no a year in revenue for IBM.

Meehan says that as far as mainframe products are concerned, "IBM has pretty much saturated the commercial market. If they want to grow by 14% to 15% a year, they have to move into the scientific and engineering side," where they can capitalize on their products and their corporate name.

PUSHED UP. Besides bringing out the 3090 Vector Facility, IBM said it was pushing up to the fourth quarter of 1986 from the second quarter of 1987 the delivery date of its 3090 model 400, the four-processor version of the new Sierra mainframe line.

When introduced [*ElectronicsWeek,* Feb. 18, 1985, p. 13], IBM's 3090 family consisted of the entry-level model 200, a $5 million two-processor machine, and the four-processor model 400, a $4.3 million upgrade to the model 200. The model 400's power is estimated at 39 million to 61 million instructions per second for general-purpose applications and at 54 to 93 mips for scientific and engineering uses.

Developed by IBM's Data Systems Division at plants in Kingston and Poughkeepsie, N. Y., the new vector product will be available in February 1986. One vector facility with frame costs $370,000; an additional vector facility costs $230,000, IBM said. *–Robert J. Kozma*

ROBOTICS

DIRECT DRIVE SPEEDS UP BOARD-ASSEMBLY ROBOTS

KOKOMO, IND.

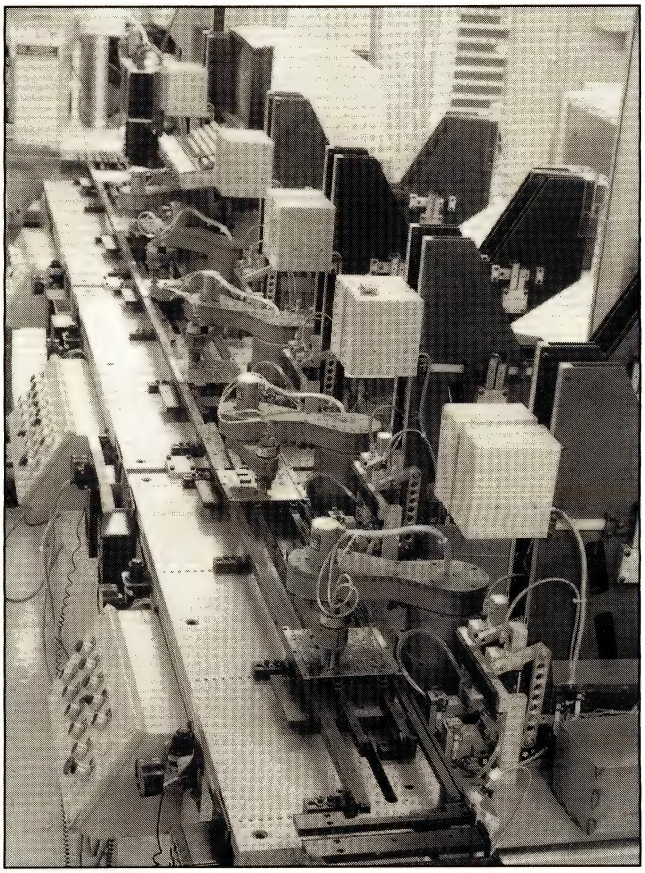
General Motors Corp. sees robot arms with direct servomotor drive as the next wave in electronics and small-assembly robots. It is about to bring to market the results of 2½ years of work on direct-drive robots, which can accurately pick and place electronic components much faster and more reliably than their gear-driven cousins.

The automaker's Delco Electronics Division in Kokomo originally designed and built direct-drive robots to meet its high-volume internal needs because no commercially available system met its requirements for speed, accuracy, and reliability [*Electronics,* July 28, 1983, p. 41]. Pushing the Delco robot technology into commercial markets is GMF Robotics Corp., Troy, Mich., a joint venture between GM and Japan's Fanuc Ltd., with which Delco has set up a separate joint-development program.

Direct-drive systems promise higher reliability and faster high-accuracy movement because they do away with mechanical gearing, and so don't suffer from the varying torque outputs seen with conventional robot motors, vendors say.

In June 1984, Adept Technology Inc., Sunnyvale, Calif., was first to market with a robot driven directly by brushless dc servomotors, called AdeptOne. Adept now claims nearly 300 AdeptOne robots shipped. Now a bevy of robot vendors is planning to introduce direct-drive automatons of their own. Some eight commercial robot vendors exhibited prototype direct-drive arms at the September International Symposium on Industrial Robots in Tokyo, including Panasonic, Fanuc, Kawasaki, Yamaha, and Dainichi Kiko.

Adept specifies its pick-and-place cycle time at 0.9 seconds, some five times faster than most conventionally driven robot arms.



FIVE-HANDED GAME. Delco's direct-servomotor-drive robot system has five arms for placing five components on boards every 3 seconds.

"Part of this is marketing and part of it is real," observes analyst Laura Conigliaro of Prudential-Bache Securities Inc., New York. "Direct drive does offer benefits. But because Adept is using it very visibly in their marketing and because Adept happens to be doing pretty well, everybody and their brother is now looking at this feature. What we'll probably see is a half dozen Japanese companies making families of direct-drive robots, and a lot of the vendors here will buy them and incorporate them into their lines."

The direct-drive arm developed by Delco engineers is in use on a modular, five-arm, vision-equipped system on the production floor. GMF plans introduction as soon as early next year of a new family of direct-drive robot products.

EYE OPENER. "When we saw which way they [Delco] were going, it opened our eyes to the potential for direct drive," says Guy W. Potok, GMF's vice president of engineering. "Delco has helped us determine what the requirements for the market are going to be."

"When we started out on this thing, there was absolutely nothing on the market that came close to what we needed in speed and accuracy," explains Earl E. Harmes, Delco manager of equipment and tool development. Though several commercially available arms could meet Delco's accuracy requirements, most had cycle times in the 8-s range, not fast enough for Delco's high-volume automotive electronics applications.

In production use since August, the direct-drive Delco robot is being used by the division to surface-mount integrated-circuit flat packs on a computer board for fuel and ignition control. The system places nine packages with ±0.001-in. accuracy on a 5½-by-8-in. board, working at two robot-arm cycles per board. Thanks to a speedy 1.5 s pick-and-place cycle time, with board station-to-station indexing accomplished transparently during the fetch portion of the robot cycle, this means the system spits out a board with nine more parts on it every 3 s. The boards then go on to high-speed surface-mounting equipment from Philips, Eindhoven, the Netherlands, which places the passive components.

Besides the performance improvement of direct drive, Harmes notes that better reliability in high-volume applications was another major incentive for design of the Delco arm. Delco is building a second, more refined version of the original five-armed system that the division plans to have in production use beginning next March. That system has already "been put through millions of cycles without a failure" in tests performed at the General Motors Technical Center in Warren, Mich., Harmes says.

The 10-in.-high Delco arm has a 14-in. reach and a 4-oz payload capacity. It is a Scara (selective-compliance assembly robot arm) design that relies on Rockwell International Corp. 65C02P2 8-bit microprocessors to control two of three dc-motor-driven axes.

The first of the initial system's three modules is equipped with an arm and a home-grown Delco vision system for obtaining alignment coordinates, which differ from board to board. The coordinates are passed on to controllers in the second two modules, each of which is equipped with two arms. Overall system control is provided by a Modicon programmable controller.

'Delco opened our eyes to direct drive'

The forthcoming GMF family will include direct-drive arms of various sizes, including robots for surface mounting, IC handling, and discrete-component placement, says Potok. At least some of the GMF line will be manufactured by Fanuc in Japan. A forerunner was visible at the recent Tokyo show, where Fanuc showed a prototype direct-drive arm based on a design "conceived at GMF and developed by Fanuc under our supervision and review," Potok says.

Although it draws heavily on technology from the Delco system, the GMF family will feature a modular design based on common components, including 68000-based controllers for better versatility and higher performance than the Delco system, Potok says. "We expect that we will be more than competitive," says the GMF official of the coming commercial direct-drive robot wars. "We'll be offering higher performance than what's currently available, from Adept or anybody else." *–Wesley R. Iversen*

GRAPHICS

TV PROJECTOR MAKERS SHIFT AIM TO BUSINESS

NEW YORK

Large-screen projection video may no longer be a novel piece of family furniture, but it hasn't exactly become a top-selling consumer item, either. Perhaps in response to the disappointing home market, two big names in video products, Sony Corp. of Tokyo and Pansonic Industrial Co., of Secaucus, N. J., have introduced projectors aimed at new turf: corporate and educational markets.

The projectors—up and running at Video Expo in New York last week—can be hooked simultaneously to personal computers and video cassette recorders. They can be configured to allow superimposition of computer graphic images over a moving videotape or disk image.

Sony's VPH-1030Q1 has a resolution of 900 lines and is priced at about $8,600. Panasonic's PT-101 has an 800-line resolution, and is priced at about $5,300. These models go up against the ECP 2000, a similar projector already on the market from Canadian Electrohome Ltd. of Kitchener, Ontario.

Kukio Tosa, manager of product planning at the Sony Communications Product Co. in Park Ridge, N. J., says Sony intends to produce more than 10,000 units for 1986—60% to 70% of which will be sold in the U. S.

James L. Greenwood, an eastern region marketing manager with Panasonic, says his company has not established firm sales quotas, mainly because there is "very little data" about the potential market. Yet he predicts "consistent, ongoing sales" because of the vast number of computers in use in offices and schools.

ENTRENCHED. Raymond Boggs, a video product research consultant at Venture Development Corp., the Natick, Mass., market research company, is not quite so sure there is a strong market for such projection devices.

Boggs says the products have a tough challenge ahead to "replace presentation devices that are well-entrenched." Moreover, he adds, because most conference rooms are not equipped with computer terminals, installation of such systems "would require a greater commitment on the part of the user than simply buying the unit and installing it."

The Sony and Panasonic models have three projection lenses side by side. The Sony unit has three 5½-in. cathode ray tubes—red, green, and blue—behind those lenses, and Panasonic's PT-101 has three 7-in. CRTs and color lenses. Electrohome's unit has one lens, with the images from three 5-in. CRTs combined inside the unit before projection.

Sony's machine boasts easy hookup to computers and VCRs; all it needs in most cases is a cable. Panasonic's PT-101 can hook up to many microcomputers, including most Apples, the IBM PC and compatibles, and NEC machines, but needs a separate interface box.

Superimposition of RGB-2 signals over a moving video image is possible only through the use of special computer software to control the images fed into any of these projectors.

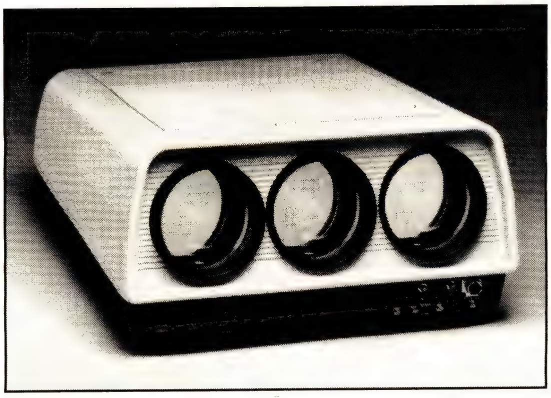
Sony had its projector on display with a screen about twice the size of Panasonic's. Even with a much larger screen, the Sony image was somewhat sharper, but Panasonic's was brighter.

MULTISCAN. A major feature of Sony's projector is a multiscan capability, which allows projection of screen images from most micro-, mini-, and mainframe computers, automatically locking onto the scan signal. The multiscan system is essentially the same one Sony used in an earlier monitor [*Electronics-Week*, Oct. 8, 1984, p. 34].

Sony's multiscan technology overcomes some pretty fair stumbling blocks for projection of computer images. Unstandardized, the horizontal and vertical scan rates of different computers can vary considerably.

"Every computer [type] has different horizontal-scanning signal-frequency characteristics," says Sony's Tosa. "With current projection TVs you have to adjust projectors internally almost every time you want to connect a different computer. It's a headache." Sony's multiscan technology includes a frequency-to-voltage converter and automatic locking circuitry to counter that problem. The machine can then identify the voltage and automatically lock it in for steady registration. A manual registration control allows the user to realign the image on its screen without moving the projection unit.

Though still unable to handle the full range of scan rates, the Sony model features a "scan-rate window"



AUTOMATIC SCANNING. Sony's new projector automatically locks onto the scan signal from most computers.

that allows the unit to accept scan rates ranging from 15 kHz to 26 kHz horizontal and from 50 Hz to 100 Hz vertical. Sony says the projector connects with about 80% of current computers by plugging in a standard RGB-1 or RGB-2 connector.

THE COMPETITION. Sony and Panasonic are not the first to come up with machines that will project computer and video images. Nor is Sony the first to make computer hookup easy.

Canadian Electrohome offers its ECP 2000, which has a resolution of 1,200 lines, for about $14,000. A video unit can be hooked to it simultaneously with a computer and it will project an image up to 168 in. diagonally (Sony's goes to 200 in.). Electrohome's unit does not offer automatic scanning, but it will hook up directly to any computer that puts out either an RGB or a composite signal.

Simultaneous display—without projection—has also hit the market before. Digital Equipment Corp., Maynard, Mass., sells an Interactive Video Instructional System (IVIS) that can simultaneously display computer and video images on a monitor. IVIS is designed for individual use, but one user reports hooking it up to a TV projector.

–Tobias Naegele and John F. King

MICROPROCESSORS

INMOS FINALLY UNVEILS THE 32-BIT TRANSPUTER

LONDON

At the transputer's long-awaited launch, staged in London, New York, San Francisco, and Tokyo last week, Inmos International plc added substance to its claim that the transputer is the first microprocessor suited to parallel-processing architectures.

Inmos released performance benchmarks that put the transputer, which is based on a reduced-instruction-set computer architecture, ahead of any other microprocessor announced so far, and it showed two working hardware systems. It introduced three transputer-evaluation boards and two interface chips that help connect the transputer to systems based on other microprocessors. And the company outlined development plans, among them a second-generation transputer with an on-chip floating-point multiplier.

In assuring customers that samples would be ready by the first quarter of 1986, Inmos said transputer production at its Newport, South Wales, plant now runs at 1,000 wafer starts a month. Current production is going into board-level development products, which are on sale now.

The first transputer, the 32-bit T414, has a 50-ns cycle time and executes about 10 million instructions per second. Inmos says the 76-mm^2 chip runs high-level-language programs some 4 times faster than a Motorola 68020, 9 times faster than an Intel 286, and 12 times faster than a National Semiconductor 32032. On single-precision floating-point operations, it is 15 times faster than a 68020 and 20% slower than a 68020 with a coprocessor.

But what makes the transputer radically different from other microprocessors is its 2-K bytes (4-K bytes in a version due next spring) of on-chip memory and its four asynchronous communications channels, which have a combined data-communications capacity of 5 megabytes/s. These two features support the transputer's ability to work efficiently in large arrays [*Electronics*, Nov. 17, 1983, p. 109].

The communications channels form transputer-to-transputer links, with which the system designer can spin a web of cooperating processors. The network of links, which replaces a shared bus, lets a system execute at thousands of mips, Inmos claims.

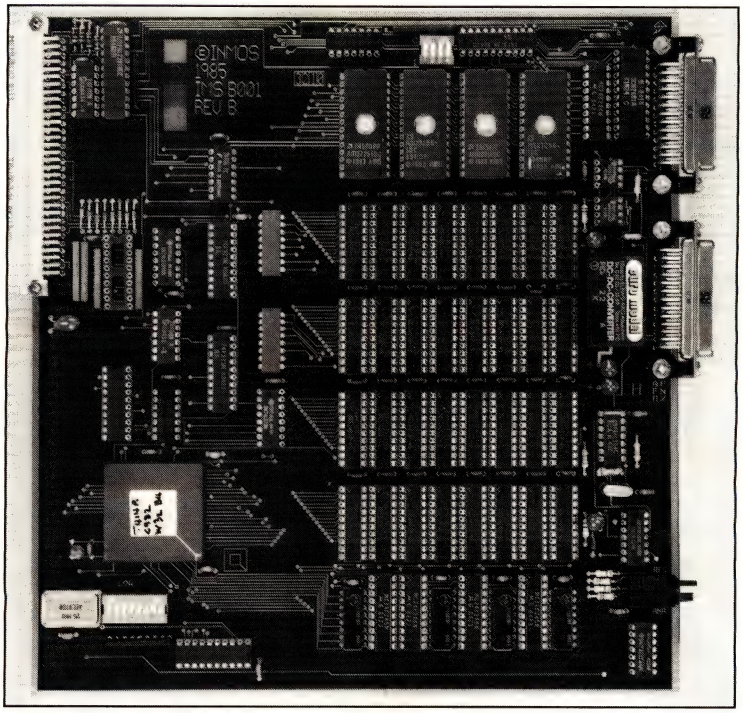
LINEAR GROWTH. To demonstrate that adding transputers can increase performance in proportional increments, Inmos had a 100-mips system with 10 transputers running a graphics application. Company personnel switched in different numbers of processors to show the change in speed. A prototype of Meiko Ltd.'s Computing Surface, which uses 16-bit transputers and delivers around 500 mips, was also running at the Inmos introduction (see story, p. 43).

More than two years ago, Inmos introduced its Occam language for parallel processing and software-development systems for the language. The new transputer boards can execute Occam programs written on those systems.

First to go on sale are three boards for the T414. Each board comprises one transputer; bootstrap firmware; 64-K bytes, 1 or 2 megabytes of random-access memory; and two RS-232-C ports. The transputer's communications channels are accessed through edge connectors, so the cards can be linked to form an array. A board carrying several transputers is in the works.

Next month, Inmos will unveil development software and an evaluation board for use with the IBM Corp. Personal Computer and PC AT. The software runs on a system with 640-K bytes of RAM and a hard-disk drive. The board, which carries a T414 and 1 megabyte of RAM, plugs into a PC expansion slot. Inmos also expects to introduce Fortran, Pascal, and C compilers by mid-1986.

The two link-adapter chips introduced last week complete one end of a transputer communications channel when interfacing to a microprocessor bus or to a serial link. Two of the chips can be connected back-to-back to form a complete Occam channel. The chips can also be teamed with another processor to emulate a transputer—but, warns Peter Cavill, director of microcomputer products, the emulation would be very slow. The C001 connects the Inmos serial link with two byte-wide interfaces, one for input and the other for output. The C002 ties a transputer channel to a



TRYOUTS. The IMS-B001-1 is one of the evaluation boards that carry Inmos' transputer, a processor chip designed for parallel-computing systems.

conventional microprocessor bus.

Under Douglas Stevenson, Inmos's new chief executive, transputer manufacture is the top priority of Inmos's Newport plant. A process variant has been developed at the firm's Colorado Springs plant specifically for the transputer. A further process refinement, adding selective-metalization capability, will shortly be phased in to allow Inmos to make smaller memory cells. It will be used to make the T424, the 32-bit transputer with 4-K bytes of on-chip RAM that is due by mid-1986.

PLANS. Inmos plans to introduce a 16-bit transputer and a disk controller during the first quarter of 1986. The disk controller is a transputer-based chip that lets a user set up the disk's data-blocking scheme and choose his own error-correction protocols. "We can snip off the [software] process running the file handling and run it in the disk controller itself," says Ian Pearson, director of microcomputer operations.

And Inmos is just starting the design of a second-generation transputer. The company is completely reengineering the RISC processor to obtain a 30% shrink and 30% speed increase. The freed silicon area will be used to add a floating-point multiplier and a small processor for link-control functions. "We are able to reengineer the processor because we have never released its instruction set," says Cavill. "The only interface we present to the customer is a high-level language such as Occam, C, or Pascal." The new chip is scheduled to arrive in the the first quarter of 1987.

Transputer production has top priority at new South Wales plant

Whether the world is ready for the transputer remains a question, but there are some noteworthy straws in the wind. In addition to the system from Inmos spinoff Meiko, the transputer already figures in the European Esprit project and Britain's Alvey fifth-generation computer effort. Plessey's Roke Manor Research Establishment and the Royal Radar Research Establishment are enthusiastic about the transputer for military signal processing.

At least one company is evaluating the transputer for factory-automation applications, Inmos officials say. And one small consultancy, Smith Associates Ltd., Cobham, Surrey, is using it in an automatic fingerprint-recognition system. The system comprises an array of 100 transputers teamed to a disk subsystem and is reported to achieve a nominal execution rate of 5 billion instructions per second. *–Kevin Smith*

DATA ACQUISITION

ADC USES ONLY 16 mW TO RUN AT DIZZYING 1 GHz

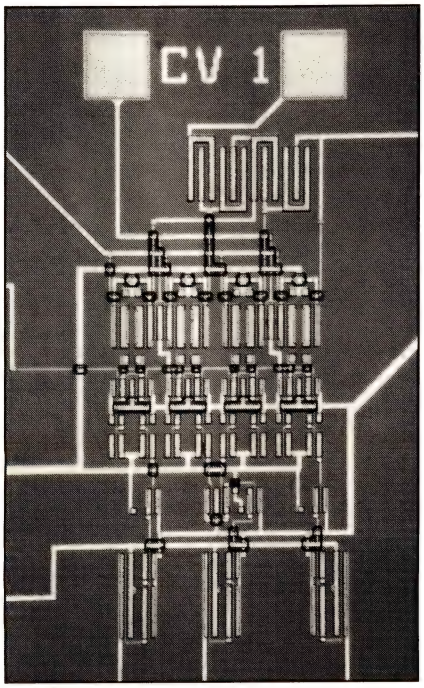
LIMEIL BRÉVANNES, FRANCE

A 2-bit analog-to-digital converter from the Laboratoires d'Electronique et de Physique Appliquée (LEP) could lead to a leap in performance for future digital-signal-processing systems. The gallium arsenide chip runs at 1 GHz and consumes a mere 16 mW.

The LEP, the principal French research laboratory of Philips, the Netherlands, set out to develop the converter because its engineers were convinced that the present capabilities of data-acquisition circuits would limit the performance of future generations of signal-processing systems as well as telecommunications, oscilloscopy, and radar systems. All these applications will soon require ultrahigh-speed medium-resolution ADCs, they say.

SPEED LIMIT. The snag is that though 8-bit ADCs are already available in silicon, their speed is limited to about 100 MHz—just one tenth the speed necessary for the applications in question. GaAs is fast enough but has been found wanting on two other counts. First, GaAs comparators tend to have low sensitivity. Second, operating in the gigahertz range, their power consumption has so far been prohibitively high. Both these factors combine to limit their resolution to only a couple of bits.

Thierry Ducourant, the LEP engineer coordinating the project, believes his team has found a way to increase sensitivity and lower power consumption. The laboratory's experimental ADC, though currently implemented as a 2-bit circuit, was designed so that it could be expanded to the 8-bit resolution needed by practical applications. Officials of the research facility will not discuss how it is possible to expand the resolution, nor will they talk about commercial products that might result from their work.



QUICK SAMPLE. LEP's 2-bit analog-to-digital converter has an original comparator design, operating at 1 GHz and dissipating 16 mW.

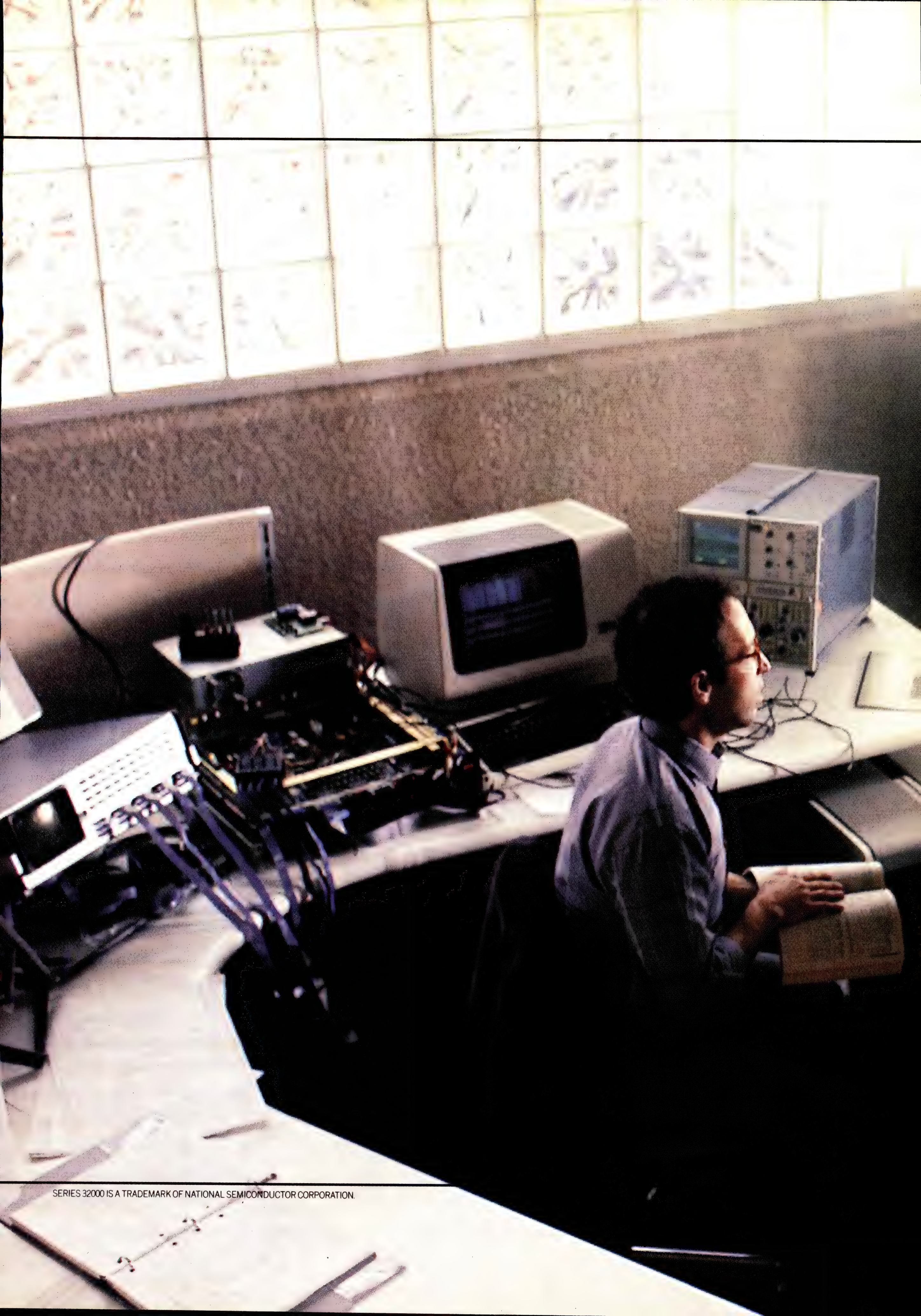
The LEP's technology features FETs with 1-μm gates and 4-μm drain-source spacing. Changing from the more commonly used normally-on, or depletion-mode, FET technology to the LEP's normally-off enhancement-mode process achieved a dramatic decrease in power dissipation, claim the LEP researchers. This results mainly from the elimination of parasitic effects that plague depletion-mode circuits and result in intolerably high hysteresis.

SINGLE CLOCK. LEP engineers solved the sensitivity problem by coming up with an original comparator design that provides sensitivity of ±10 mV at 1 GHz per comparator. The ADC uses four comparators (a converter with a resolution of n bits requires 2^n comparators) in a parallel structure. Central to the design of each comparator is a wide-band, low-gain amplifier that amplifies the difference between the input signal to be digitized and a reference voltage.

A flip-flop controlled by an external clock is inserted in each amplifier for synchronization purposes. The single clock simultaneously activates the comparators whose flip-flops are in the enabling state. The activated circuits compare the input signal with four reference levels implemented by means of a simple resistive ladder.

This architecture, essentially a sample-and-hold circuit, avoids the pitfalls of the standard semiparallel two-clock architecture. The two-clock approach splits operation into two successive conversions, each providing half the desired resolution. But an increment of time and some sensitivity are lost in each conversion, a disadvantage the single-clock LEP circuit does not share.

At 1 GHz, the converter matches the speed of the only other similar circuit on which results have been published, that of RCA Corp. But the LEP chip far outdoes RCA's in power consumption. RCA's 2- and 3-bit converters, reported in 1983, consume between 150 and 200 mW per bit. *–Robert T. Gallagher*



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"I can tell by the look on your face. You've been talking to marketing about the new system again."

"How're we going to do it if you have to create memory management and floating point units out of thin air?"

"That's not a problem—"

"On time and on budget?"

"We're going to use a complete 32-bit chip set—"

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"Can we start today?"

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Of all the available 32-bit microprocessors, only one delivers supermini performance from a chip set you can work with today. Series 32000™ is the world's most complete 32-bit microprocessor family, with CPU, MMU, FPU, TCU, ICU and DMA controllers in place right now.

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THE SUPERMINI ON A CHIP

Circle 23 on reader service card

OCTOBER 7, 1985

ELECTRONICS WEEK

BAUSCH & LOMB SELLS DIVISION . . .

Bausch & Lomb Inc. has apparently finished divesting itself of its industrial-instruments businesses a year after it initiated a campaign to focus on medical and laboratory markets. The final twist to the spinoff involves Houston Instrument, a manufacturer of plotters and digitizers. Bausch & Lomb is selling the Austin, Texas, company to Ametek Inc., New York, for $46 million. Houston Instrument, founded 26 years ago and acquired by Bausch & Lomb in 1967, employs 425 workers in Austin. The Rochester, N. Y., optical company has sold four other industrial-instrumentation operations that produce industrial controls, scanning electron microscopes, and analytical equipment.

. . AS BUYER SEEKS HIGH-TECH NICHE

Ametek, a manufacturer of electrical motors and industrial scientific equipment, is trying to position itself in the mainstream of new high-tech markets through a series of acquisitions and new-product developments. Earlier this year, Ametek bought Panalarm Co., a maker of industrial instruments in Chicago; Carsonite, a producer of composite materials in Carson City, Nev.; and Orionics, an optical-fiber test-systems company in Bozeman, Mont. In late August, Ametek's engineers in Pasadena, Calif., demonstrated a parallel-computing system that can link up to 64 processing nodes.

CBEMA SEES RISE IN 1985 REVENUE

The Computer and Business Equipment Manufacturers Association, Washington, forecasts an increase in revenue from data-processing equipment and services during 1985. The CBEMA says revenue from the sale of computers and related equipment and services and the sale of software and related services will increase by 11.5% to $141.7 billion in 1985, up from $127.1 billion in 1984. Computer equipment and services should rise 10% to $101 billion, from 1984's $91.8 billion, as software and related services jump an estimated 15.5% to $40.7 billion in 1985, from $35.3 billion last year. The CBEMA also predicts that microcomputer sales will rise by 10% in 1985 to $8.5 billion, from $7.9 billion, as minicomputer revenue increases 11% to $4.7 billion, from $4.2 billion in 1984.

NYNEX AND NTT TO SWAP EXPERTISE

Two newly privatized telephone companies—Nynex, of White Plains, N. Y., and Nippon Telegraph & Telephone Corp., Tokyo—have signed a statement of intent to share each other's marketing expertise. A previous memo signed by the two telecommunications giants last July called for a personnel and information exchange program. This has now been further defined as a trial exchange of marketing representatives and mutual assistance in evaluating products, equipment, and services, and in assessing worldwide marketing opportunities.

MICRO OUTLOOK BRIGHT IN EUROPE

The European electronics industry can expect steady growth in the low-end microcomputer hardware and software market through 1990, according to a study by Frost & Sullivan Inc. The New York market research company says that the hardware market will be worth $6.93 billion by 1990, more than double this year's $3.079 billion. Software sales in Western Europe for low-end microcomputers could reach $6.87 billion in 1990, a big increase over this year's $1.297 billion. The study predicts a strong Japanese challenge in the home and small business computer sectors of the market with the introduction of second-generation machines. It also predicts that the educational segment will grow at a much faster rate than will the small business and home/hobbyist segment.

AT&T TO SUPPLY ATEX HARDWARE

AT&T has reached a tentative agreement to supply hardware for the next generation of computer publishing systems from Atex Inc., a Kodak subsidiary in Bedford, Mass. In the next few months, the signed letter of intent should lead to a long-term multimillion-dollar contract under which AT&T will supply software, networking products, and both fault-tolerant and general-purpose computers. The agreement covers both current and future products.

RISE SEEN FOR CHEMICAL SALES

Free-world consumption of electronics chemicals and materials will reach $15 billion in 1989, up from about $8 billion in 1984, according to a study by Charles H. Kline & Co., a Fairfield, N. J., market research company. This equals an average annual growth rate of 14% over the next five years. The U. S. will remain the largest consumer of these raw materials—14 major product categories including organic and inorganic chemicals, polymers, and metals. But as a percentage of the total demand, U. S. consumption, estimated to rise from $4 billion in 1984 to $6 billion in 1989, will decline relative to the rest of the free world. Domestic demand by 1989 will represent 42% of the world total compared with 47% in 1984. Japanese consumption of electronics chemicals and materials will rank second at $5 billion in 1989 (32% of the total), compared with $2 billion last year. Although Southeast Asia currently ranks last in demand for these products at $700 million, it will enjoy the fastest growth rate in the free world—exceeding $2 billion by 1989.

ERICSSON QUITS U. S. PC MARKET

One year in the topsy-turvy U. S. market for personal computers is all Ericsson Inc. wants. The American operation, jointly owned by L. M. Ericsson of Stockholm and Atlantic Richfield Co. of Los Angeles, announced last week it will end U. S. sales of Ericsson's personal computer products, including a unit compatible with the IBM Personal Computer. About 175 dealers and product representatives have been signed up in the U. S. by Ericsson since 1984. None of the dealerships will be renewed after Dec. 31. Ericsson—which recently moved its U. S. headquarters from Greenwich, Conn., to Richardson, Texas—is now attempting to focus its core business strategy on American telecommunications markets. Personal computers accounted for 2% of the revenue. Ericsson, which introduced its first personal computers in 1982, will continue marketing desktop work stations in Europe.

NASA GETS SUPER CRAY

What is billed as the world's most powerful supercomputer, a Cray-2 model 2002, began operations last week at the National Aeronautics and Space Administration's Ames Research Center in Mountain View, Calif. The Cray, with a memory of 256 million 64-bit words, will be used for simulating aircraft flight. It is the first major component in a NASA system targeted to perform at the rate of a billion floating point operations a second by 1987.

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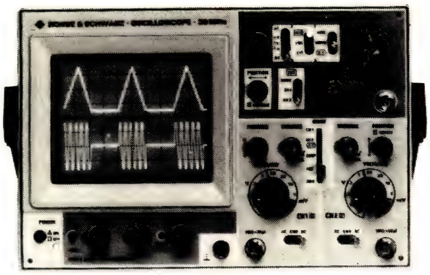

Oscilloscope BOP · DC to 30 MHz (above)
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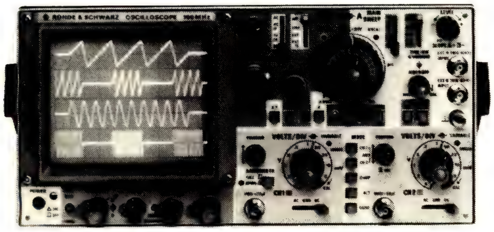

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MASSCOMP BETS ON MULTIPROCESSORS

COMPANY NEEDS TO REJUVENATE ITS MARKETING STRATEGIES AND RETURN TO HIGH-GROWTH DAYS OF THE PAST

WESTFORD, MASS.

With football teams and electronics companies, the pressure for a big play grows after three subpar quarters. So Masscomp, struggling for most of a year, recently launched a long pass downfield with the announcement of a new line of multiprocessor computers.

The company hopes its new products will accomplish two goals: rejuvenate its efforts to score big in the high-performance work-station market and resurrect the growth patterns that it sustained in its early days as a startup.

For Masscomp, as for many other electronics companies, the recent downturn in fortunes was abrupt. From its founding in 1981, the computer maker's revenue grew to $45 million in fiscal 1985, twice 1984's level.

But Masscomp's revenue declined in the last two quarters of fiscal 1985 (which ended June 29), and the company expects that revenue for the first quarter of fiscal 1986 will be no better than flat compared with the fourth quarter. In addition, it posted a loss of nearly $1.7 million in 1985's fourth quarter and will post another loss in the quarter just ended Sept. 30. In an austerity move in August, the company slashed wages and salaries across the board.

Masscomp—formally Massachusetts Computer Corp.—has attempted to create a niche in the work-station market for itself with a triple-bus architecture and an emphasis on other innovative technology. Its latest computers [*Electronics*, Sept. 30, 1985, p. 54], which contain up to four processors, extend the company's innovations into even high-performance ranges. But regardless of how technically superior new multiprocessor computers are, Masscomp will likely still face marketing problems.

Douglas Rowan, vice president of marketing, quality, and service, says the major difficulty has been differentiating Masscomp from other work-station vendors. Although Masscomp sells work stations, it targets real-time data acquisition and technical computing as its bread-and-butter markets.

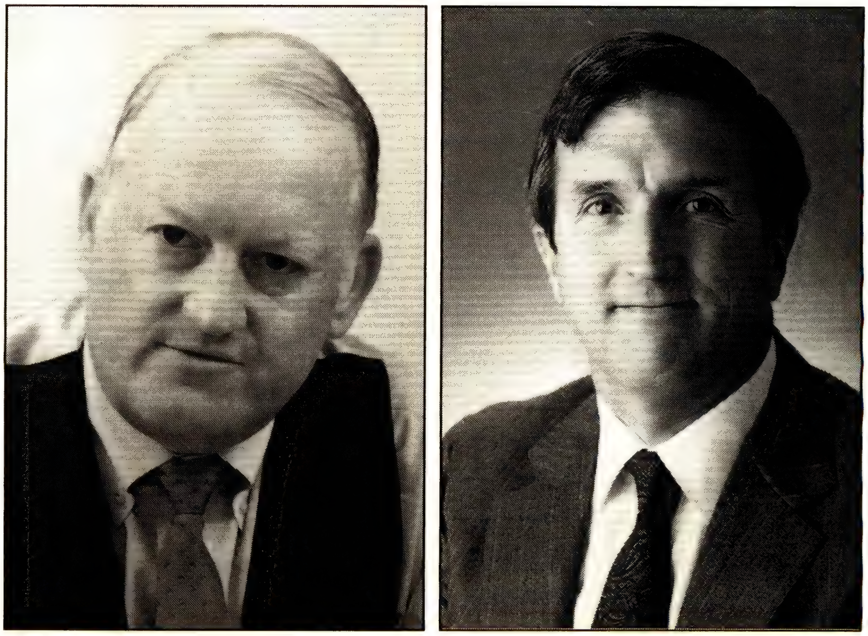
The company is also striving for a reputation as a very-high-performance or "microsupercomputer company." At the top end of the new line of machines, Masscomp claims to offer 10% of the performance of a Cray Research Inc. supercomputer for less than 4% of the bigger machine's price. Masscomp says the same system, which includes four Motorola Corp. 68020 processors, will also outperform a Digital Equipment Corp. VAX 11/780 for less money.

Whether those performance levels can be achieved is one issue, but it is unlikely that performance itself can rescue Masscomp from the "JAWS" syndrome—that is, being perceived by customers as "just another work-station" vendor. "If they want to compete [in technical computing and real-time markets], they have to stop getting people to say, 'Sun, Apollo, and Masscomp,' " says Adam Zais, a program manager at market researcher International Data Corp., Framingham, Mass. "They need somebody to paint a picture of themselves as the hot-box guys."

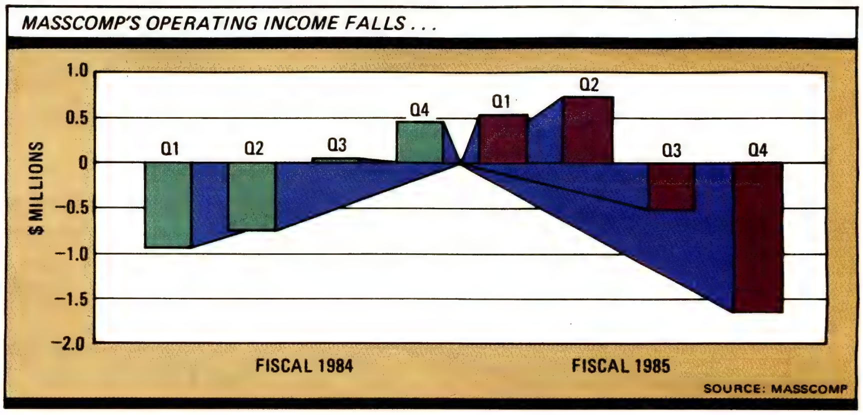
In fact, building high-performance machines for its market niche has been Masscomp's idea from the beginning, says Lorrin Gale, vice president of engineering and a company cofounder. Before the founding of the company in August 1981, venture capitalists, through some intermediaries, approached Gale with the idea of building a laboratory Apple-type machine costing about $15,000. But he had another idea.

SERIOUS BUSINESS. "What I wanted to build was a more serious machine for the man who had $50,000—a beefier product," says Gale. The idea arose because he believed the major minicomputer makers had begun to move away from that market in their strategic focus. Machines designed to serve a broad array of users can't provide the performance of specialized real-time data-acquisition computers, Gale says. Some major vendors dropped out of the market completely, while others made it a

OPTIMISTIC. Masscomp president August Klein (left) and vice president Douglas Rowan hope the new line of multiprocessor computers will lift the company out of its financial doldrums.



MASSCOMP'S OPERATING INCOME FALLS . . .



SOURCE: MASSCOMP

minor part of their business.

Building a higher-range—read more expensive—machine actually requires less startup money, says Gale. “To build a good low-end machine requires lots of capital to get the price down. In a mid-range machine, you're selling the intellectual content—what you're selling is ‘goodness’ rather than low cost.”

When Gale, who was an operations manager and worked on advanced development and planning at DEC before co-founding Masscomp, presented these thoughts to the venture people, “They shrugged their shoulders and said, ‘Okay, whatever you want to do is okay with us,’ ” says Gale. Three rounds of venture financing brought the startup more than $16 million. And a public offering in August 1984 generated over $37 million.

On the product side, Masscomp shipped its first system in November 1982 and its 1,000th system last May. The customer base is divided equally between end-users and over 70 original-equipment manufacturers. “Our basic strategy was to sign up a lot of little companies,” says Klein, “hoping that a number would be successful. We've suffered from that in this environment. Some have not grown as anticipated, but interestingly, none has failed.”

> *New computer outperforms VAX but costs less*

By this past summer, however, salaries for all 540 of the company's employees were slashed by between 6% and 12%, depending on level. Klein chose wage cuts rather than layoffs because they provide more immediate cost savings and because he wants to keep people in place for production in the event of a business upsurge. One official reports that no one has yet left Masscomp as a result of the salary cuts, perhaps partly because the company also offered stock options to all employees at the time of the salary cuts.

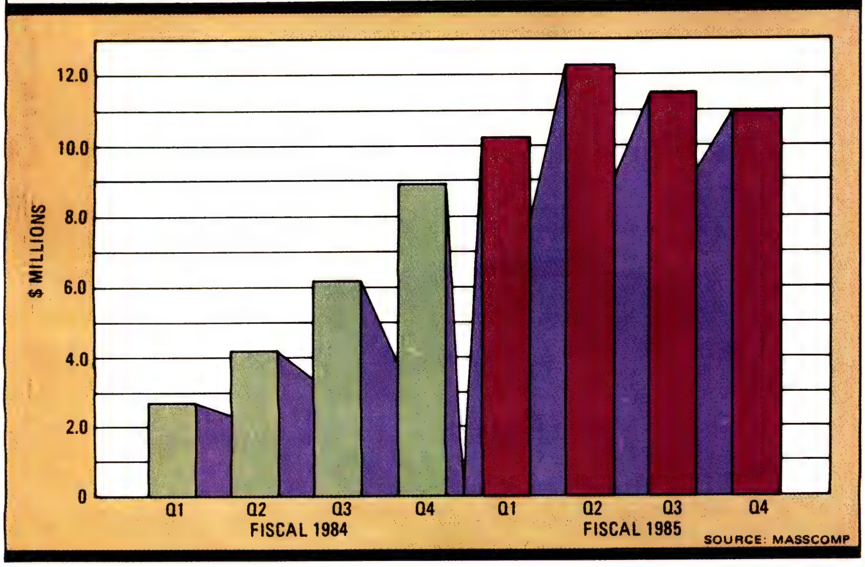
Klein attributes Masscomp's expected loss in the quarter to the expense of developing new products and the general downturn. But he also says that one of the problems with the computer business currently is that customers are waiting for new products. So he has high hopes for the company's new multiple-processor machines.

GROWING ABROAD. International operations are another source of optimism for Klein and his crew. With Masscomp operating abroad for only 18 months, the overseas market is now responsible for 8% of company revenue, all of it in Europe. Masscomp recently began operations in Japan and reports that business there is off to a good start. It projects that international sales this year will rise to the 10% to 12% range, with 2% coming from outside Europe.

And as a company that prides itself on reliability, Masscomp is crowing these days about beating out a manufacturer of fault-tolerant computers in a recent competition to sell computers to the U. S. Patent Office.

But the company's current difficulties meant that the development of a new line of computers entailed more than the usual number of risks, both financial and technical. Masscomp's engineering development schedule, for example, was set to coincide precisely with the planned availability of new processors. Masscomp shipped its new systems to beta sites in August only two weeks after getting its first working chips from Motorola. “On a gamble basis, you wouldn't want to go any farther than we did,” says Gale. *–Craig D. Rose*

... AND REVENUE HAS SLIPPED



SOURCE: MASSCOMP

BOTTOM LINES

DATAQUEST SEES COMPUTER STRENGTH

Sales of business computer systems will continue to rise in 1986 and stay strong through 1987, according to a new report from Dataquest Inc. The San Jose, Calif., market research company expects worldwide sales of multiuser business computer systems to hit 516,900 units in 1986, versus 419,500 units this year. In 1984, worldwide shipments totaled 340,500. In 1987, sales should increase to 643,100 units. But the compound annual growth rate in unit shipments for the 1985-89 period will fall to 25%, compared with 35% for 1980-84.

GI SELLS OFF AGILE IMAGING

General Instrument Corp., New York, has sold its Agile image-systems technology to Computer Graphics Laboratories Inc., New York, for an undisclosed amount of cash, royalties, and stock in a subsidiary of Computer Graphics Laboratories. Agile, a computer-graphics system, features real-time interactive management of photographic images at one third to one fifth the price of comparable systems, General Instrument says. “The sale of Agile is part of our strategic program to concentrate on major businesses, reduce costs, and adjust to changes in our markets,” says chairman Frank G. Hickey.

RAYTHEON INVESTS IN DIGITAL TECHNOLOGIES

Raytheon Co., through its Raytheon Ventures operation, has obtained a minority position in Digital Techniques Inc., Burlington, Mass., for an undisclosed amount. Digital Techniques makes personal-computer-based instructional systems for use with videodisks. Raytheon, Lexington, Mass., says the move is part of its program to identify and invest in areas of emerging technology to complement its technical interests while encouraging the growth of small companies. Raytheon recently invested in Lisp Machine Inc. [*Electronics*, Sept. 9, 1985, p. 83].

OPT INDUSTRIES BORROWS $6 MILLION

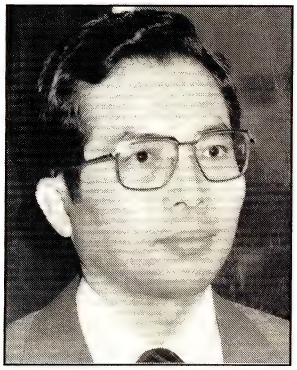
Opt Industries Inc., a maker of power supplies, filters, and transformers, completed a $6 million private placement of convertible debentures. The Phillipsburg, N. J., company will use the funds to expand its facilities and add equipment for automated testing and computer-aided design and -manufacturing.

PLAYERS

SENMOTO JOINS STARTUP, TAKES ON OLD EMPLOYER

TOKYO

Just two years ago, Sachio Senmoto was an established researcher in digital transmission and fiber optics at Nippon Telegraph & Telephone Corp., then a government telecommunications monopoly. His position was secure, his future ensured.



GLOBAL. Senmoto wants an international company.

Then Senmoto met a man who challenged him to do what is almost unthinkable for a Japanese professional: leave his job to help establish a new company to challenge the very giant for which Senmoto worked. The challenger was Kazuo Inamori, who at 27 started Kyocera Corp. and built it into a world leader in ceramics. Inamori wanted to create a private consortium to offer data-transmission services in competition with NTT in the soon-to-be-deregulated Japanese telecommunications market.

"He saw the new trend, and so did I," says Senmoto. "I was 39 years old. It was a big choice for me. It took me one month to decide." Some 225 firms led by Kyocera, Mitsubishi, and Sony are in the consortium, called Daini-Denden Inc. It will begin operations in the fall of 1987.

Senmoto, senior vice president, is at 42 one of the youngest top executives in Japan. He seems to enjoy being different. Though he was born in Nara, an ancient city with a Buddhist tradition, Senmoto, his wife, and four children belong to Japan's tiny Roman Catholic population. "It's God's will that I have done what I have done," he says.

His achievements are notable. After winning a Fulbright fellowship for graduate study at the University of Wisconsin, Senmoto earned his doctoral degree at the University of Florida and won another scholarship from the National Science Foundation. "I owe a lot to the U. S. government, and I feel an obligation to return what I have received," Senmoto says.

Perhaps that was part of the reason Daini-Denden recently agreed to purchase four long-distance digital switches from Digital Switch Corp. of Richardson, Texas, thus becoming the first Japanese company to buy central switching equipment from a U. S. maker. An obstacle was Senmoto's former employer, NTT, which has been slow to transfer specifications of its switching network, to which Daini-Denden must interconnect [*Electronics,* Sept. 23, 1985, p. 18]. But after the problem became public, NTT suddenly speeded up the process, and it now appears that Daini-Denden will have the documentation it needs in ample time to customize its American switches for the Japanese network.

NEEDED STIMULUS. Although Senmoto sees an information revolution occurring in Japan, he also notes a flaw. "The U. S. telecommunications market is growing much faster than ours. The only way to stimulate growth in Japan is for us to change our monopolistic, insular way of thinking and create some healthy competition in telecommunications services, so that only the best technology is used. That's why I left NTT."

He took several colleagues with him—"About 20 of them, mostly in their 30s, mostly engineers, and mostly elites with experience in the U. S. We're trying hard to be international. We've got to be to survive." *–Michael Berger*

AMSTER LEADS IRWIN INTO BLACK

ANN ARBOR, MICH.

It hasn't been easy for Herbert S. Amster and his co-workers at Irwin Magnetic Systems Inc., but it looks as if the company has found a niche. "We did about $12.5 million worth of business in the year ended June 30, up from practically nothing the year before," says Amster, named chairman in May. The company, which manufactures minicartridge tape-drive systems used to back up personal computer Winchester disks, turned profitable this calendar year and will have sales of more than $25 million in the current fiscal year, he adds.

As a low-cost alternative to conventional ¼-in. streaming tape drives, the minicartridge system developed by Irwin has turned into a strong business, in which Irwin now occupies the catbird seat. This success comes despite the current slump in the personal computer industry.

But as Amster can attest, the road to market leadership has hardly been smooth. In 1981, he joined the company known as Irwin International Inc., founded two years earlier by computer industry veteran Samuel N. Irwin, as vice president of finance. Amster had worked previously with Sam Irwin as finance vice president and chief financial officer at an earlier Irwin brainchild—Sycor Inc.—beginning in 1973. The 50-year-old native New Yorker, who has a master's degree in industrial management from the Massachusetts Institute of Technology, also did stints in finance and data-processing management at Raytheon Co. and Ford Motor Co.

Irwin International had been founded to produce a 5¼-in. Winchester disk drive that included a built-in backup tape cartridge. But it couldn't make the product sell, and the company turned to Ing C. Olivetti & C. as a partner. The new company didn't move enough products, and the union dissolved after nine months. Irwin Magnetics was formed in August 1983 to develop and market the minicartridge tape drives. Meanwhile, Irwin left to pursue other interests.

Under Amster's guidance, Irwin is courting additional original-equipment-manufacturing business. But last February, he pushed the company in a new direction with the introduction of free-standing peripheral versions of the Irwin drives sold through retail outlets.

The major targets are users of IBM Corp. Personal Computer/XTs and ATs. "IBM has about 60% of the business-PC marketplace, and going retail was our best way to get at those units," Amster explains. Though the first units weren't shipped until April, the retail business accounted for 15% of Irwin Magnetics' sales in the fiscal year just past and will amount to over half the company's business this year, he projects.

The company plans to introduce higher-density minicartridge drives. Beyond that, Irwin Magnetics is exploring other backup alternatives. Amster hints at what they might be when he says, "optical disks are an area that makes sense for everybody in the backup business to be looking at." *–Wesley R. Iversen*

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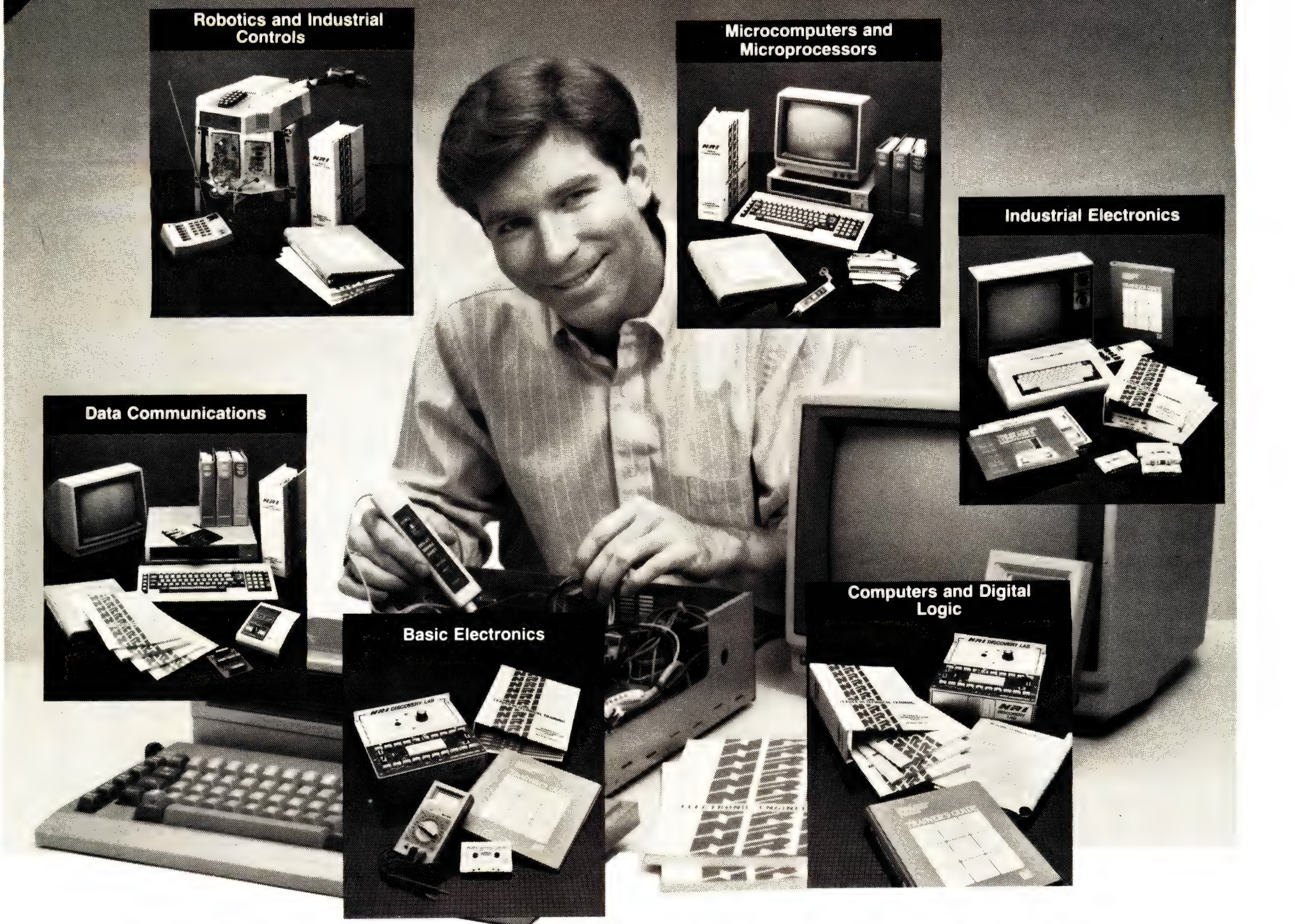
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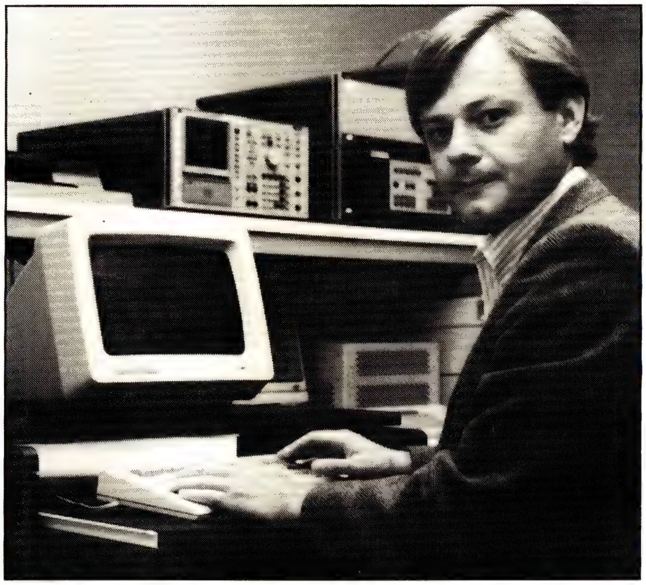
by Jack Shandle



WARY. Edward Monser of Rosemount Inc. learned that simulation can be tricky in customizing gate arrays.

NEW YORK

The complexion of the market for application-specific integrated circuits will change markedly in coming months as more ASIC vendors get into the act of guaranteeing that they can turn out prototypes of customized gate arrays fully designed on customers' work stations. They can make these guarantees because the systems houses that are their customers now can tackle the once-formidable briar patch of placement and routing.

The systems house can take on the task of making the physical interconnections for their designs because work-station makers and gate-array vendors are embarking on a new course: agreements that add the vendors' placement-and-routing packages to the design software available for the work stations.

Guarantees that gate-array vendors need not resimulate and tweak designs on their computer-aided-design systems will give customers long-sought-after control over project schedules, as well as over every aspect of chip design. However, the new freedom is not without its dangers, for systems houses are discovering that ASIC software can be tricky to work with.

A growing number of work-station makers are signing licensing agreements with gate-array vendors. These developments will boost ASICs toward achieving the rosy markets forecast for them through the 1990s.

By the end of this decade, the worldwide ASIC market is expected to reach $10 billion a year, up from $3 billion this year, says Integrated Circuit Engineering Corp. Between 1981 and 1990, the market will grow at a compound annual rate of 31%, compared with about 18% for the semiconductor industry as a whole, and will account for about 14% of total worldwide merchant IC sales, predicts the Scottsdale, Ariz., company.

Work-station makers think they are in a good position to serve the systems houses that will be developing ASICs. "There is a much higher confidence level on the part of the ASIC vendors," says Kathleen Meiners, marketing manager for semiconductor applications at Daisy Systems Corp., Mountain View, Calif. "They're coming around to the idea of work stations being able to do the job."

ASIC vendors now see work stations can do the design job

It was Daisy's chief rival, Mentor Graphics Corp., Beaverton, Ore., that signed the groundbreaking agreement in March with Gould AMI, Santa Clara, Calif., for AMI's macro libraries for arrays from 1,000 to 4,000 gates in a 3-μm double-layer-metal CMOS process.

Five ASIC gate-array vendors offer such software packages on Mentor work stations, with two or more on the way early next year, according to Bruce Farly, semicustom-product marketing manager at Mentor's Automation Products Division in San Jose, Calif. Daisy will introduce competitive kits before the year is out, Meiners says. So far, Valid Logic Systems Inc., the third major work-station maker, has not announced similar agreements.

Since Gould AMI took the plunge, Mentor has signed Array Technology, Honeywell, Mostek, and Motorola. "It's very clear the AMI agreement changed the face of the industry," Farly says. "Other vendors are showing much more enthusiastic acceptance and more interest in speeding their project development."

Once the work-station maker and the ASIC vendor reach agreement on adapting the software, responsibility for distributing and updating it rests with the vendor. Work-station makers have abandoned the concept of supporting 50 or more software packages. "We were naive in the past," says Daisy's Meiners. "There is no way we can keep on top of technology changes for all vendors."

HEADACHE RELIEF. Small to midsized systems houses, such as Decision Data Computer Corp., Horsham, Pa., and Rosemount Inc., an aerospace company in Eden Prairie, Minn., should find welcome relief to ASIC-user headaches in the new software. Though it is mostly successful, the small percentage that fails poses obstacles in the development of new products.

At Decision Data, senior engineer Max Day and his design team ran into a typical problem that ultimately caused months of delay. A particular flip-flop cell in the logic design functioned inconsistently in the prototype chip. "Under certain circumstances, its outputs weren't in the right state," he says.

The culprit turned out to be poor communications at the critical stage when the customer completes the logic design and hands it over to the ASIC vendor for placement and routing.

Day's design team was using the vendor's cell library, and when it discovered the library lacked a particular flip-flop macro, it created one from logic gates. Not recognizing the maverick macro for what it was, the vendor's placement and routing software scattered its elements all over the chip, which resulted in timing problems.

While the vendor's troubleshooters scratched their heads for a solution, the delay forced Decision Data to find another semicustom house. Luckily, this vendor's library included the needed flip-flop. Using Mentor's new design software tools, Day's team preplaced gates in a cluster to create the flip-flop during placement and routing.

FALSE SIMULATION. Rosemount engineer Edward L. Monser and his design team ran into another typical problem—"we believed the [ASIC vendor's] simulator," he explained. In Monser's logic design, an internally generated signal used to latch data into a three-state bus was also being used to clear the counter chain. In the vendor-supplied prototype, the signal cleared the counter chain before the data was latched.

A Spice simulation at Rosemount pinpointed the problem, Monser says. "Once we started distributing capacitance, we were able to predict very accurately what was happening." But isolating the problem caused a six-month delay because the array vendor suspected a bug in its fabrication process—not in the simulator.

"This really goes back to the inadequacies of work stations that were not corrected until recently," says Farly. "Initial libraries did not always have the same functionality on the work station as back at the vendor. A lot of testing has to be done to be sure you get the right result on a work station."

Besides upgrading and debugging software packages, array vendors and work-station makers had other obstacles to overcome before the prototype guarantee became a reality. One was guarding system integrity. Engineers often find ways to alter software to solve particular problems. The new kits back-annotate and resimulate to guard against inadvertent contamination.

Systems houses can run afoul of quirks in the design software

Incorporating placement and routing without requiring greater customer skills posed a major difficulty for work-station makers. "It's the last step," Farly says. "Simple, reliable place and route tools that don't require the guy using them to be a CAD specialist." ☐

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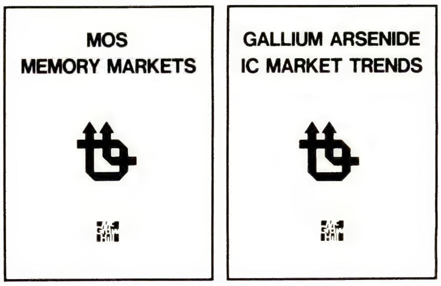

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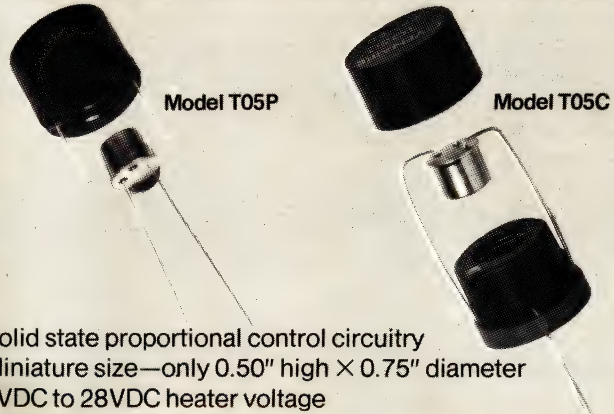

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WILL EUROPEAN MARKET OPEN FOR TELECOM SUPPLIERS?

PTTs START MOVING TOWARD DEREGULATION AND COMPETITION

by Robert T. Gallagher

CANNES, FRANCE

The winds of change are beginning to shake the European telecommunications authorities out of their accustomed ways of doing business: deregulation and open competition are coming fast. That's what participants at the annual International Televent predicted here late last month.

What is likely to result, they say, is the kind of minimal regulation of basic telecommunications networks already well under way in the U. S. and Japan, along with at least a hint of the fierce competition for equipment and auxiliary services that is the rule in those countries. To grease the competitive skids, European nations are beginning to cooperate on setting standards.

The object of the three-day get-together was to explore recent developments in world telecommunications and how to finance new add-on equipment such as call forwarding and private branch exchanges. Participants are drawn overwhelmingly from private industry and investment banking, and they tend to favor free enterprise. They clearly would like to see Europe's highly regulated telecommunications markets move in the direction of the markets in the U. S., Great Britain, and Japan.

There was a general feeling that increasing efforts to standardize telecommunications products would force European countries to join in the international competition—for equipment or services tacked onto the basic network—or else condemn their domestic infrastructures to increasing obsolescence. Only the basic European national networks, they reason, are likely to escape increasing liberalization.

Robin Bomer, director of Government Relations for British Telecom welcomes the move of PTTs (postal and telecommunications authorities) away from regulation and toward standardization. He thinks the cause is fundamental changes in information technology.

"The approach of the PTTs may be [highly regulated], but up until a few years ago, they were commendably successful in balancing the interests of consumers on the one side with the interests of manufacturers on the other side, while at the same time satisfying the perceived social, commercial, and infrastructure needs of their countries," explains Bomer.

He thinks that now, however, the boundaries of the PTTs' service monopolies are being eroded by the increasing need of commerce and industry to control large, technologically sophisticated, private and shared networks. Adding to the PTTs' woes are the emergence of outside computer-based value-added services and managed-data services, as well as cheap but increasingly effective attachments and PBXs.

If the key words of the conference were "competition," "deregulation," and "liberalization," there was no small amount of disagreement on just how to define those terms. "We're always talking about how the U. S. market is one that is now based on deregulation and competition, but it isn't," asserts Torsten Larsson, deputy director general of the Swedish Telecommunications Administration. "What has in fact happened is that the old regulations have been replaced with new ones so that what we see is a state of regulated competition." This shifts the question facing Europe from whether or not to deregulate to what degree of regulation would be optimal and appropriate, he says.

Conference participants were nearly unanimous in thinking that the European governments would draw the line at giving up any con-

trol over their basic national networks. The only exception is Britain, where the government has made what Larsson calls a political choice to establish Mercury Communications Ltd. as a competitive alternative to a privatized British Telecom. But even here, there was much doubt as to how much competition that will engender.

The U. S. market will evolve within the next several years to a "situation of oligopoly, resembling that of the U. S. automobile industry in the 1960s, with three and a half companies controlling the market" and only two producing a reasonable return on investment, says Robert Snedaker Jr., president of United Telephone Systems Inc., a U. S. supplier of telecom services.

That being the case, say some conference participants, it would be out of the question for the British market to support more than the competing British Telecom and Mercury networks. And the only other European countries that are large enough to justify competing networks would be France and West Germany. Officials for the telecommunications authorities of those two countries denied any intention of opening competition at the level of the national network, calling it a natural monopoly.

This means that outside Britain competition will be limited to suppliers of ancillary equipment such as PBXs and value-added services. The outlook in both these areas, however, looks bright since some markets already are open. For example, Jean Grenier, director of international affairs for the French Direction Générale des Télécommunications (DGT), argues that his country's market for telecommunications equipment has been "completely open" since the 1970s, for any manufacturer's gear capable of passing the DGT's muster.

Europeans are cooperating on telecom specs

Grenier's declaration, however, would make most foreign equipment suppliers snicker, since European governments, almost without exception, are constantly being accused to varying degrees of using their domestic normalization processes as a way of discouraging foreign competition.

POLITICAL PROBLEM. In the past, many foreign suppliers have found it impossible to get equipment approved with any degree of consistency for use in European countries for two reasons. First, norms have differed from one country to another to such an extent that meeting each nation's standards has required substantial adaptation of a given product. Second, in cases where there was an existing or planned domestic product, normalization requests by foreign suppliers were often met with politically motivated foot dragging.

But those days are all but over, say European government officials. What has changed, they say, is that all European governments are now committed to a process of Europe-wide normalization that would effectively dismantle national barriers. "We support equipment specifications that are common to all European countries," asserts Grenier.

COOPERATION INCREASING. Although experienced observers of the European telecommunications scene might well react with skepticism to this scenario, there are already concrete indications that it may well come to pass. The first is that cooperation among European telecommunications agencies—pushed by the European Communities—has already improved significantly. "Europe's PTTs are cooperating as never before," observes British Telecom's Bomer.

The fruit of this cooperation is that the equipment-certification process in most European countries is already being shortened from 23 months to only two, says Michel Carpentier, director general of the EC's Task Force for Information and Telecommunications Technologies.

Further, the procedure for setting a Europe-wide norm in the Conférence Européenne de Postes et Télécommunications (CEPT), the association of European PTTs, has been streamlined so only a majority vote is necessary where unanimity was required. An important point is that because CEPT includes the PTTs of countries not represented in the EC, its certification is genuinely Europe-wide. The EC is also moving to give CEPT more legal muscle to enforce standards.

Another EC initiative will probably standardize the technical requirements for telecom services "in the not too distant future," says Tjakko Schuringa, director of the EC's Telecommunications Task Force. He also expects to see common policies and joint ventures between PTTs and outside suppliers for the provision of long-distance and value-added services.

This is not to say that European governments apologize for taking an important role in determining their telecom policies. "My country is competitive internationally in four industrial fields—in nuclear generating equipment, air transport, earth transport, and telecommunications," says France's Grenier. "And these are all areas that in France are highly regulated." The message here is that Europe's governments may well take a more liberal view to telecommunications competition in the future. There is little chance, however, that they will evolve to the point of laissez faire. ☐

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Ambitious research and development programs and strong exports keep technology moving ahead

West Germany's electronics industry has remained one of the country's brightest performers. Last year, it registered sales of $45.22 billion, exports of $20.05 billion, and employed 921,000 people. In fact, it ranks first of all European industrial sectors in terms of net added value. And the outlook for the near future remains optimistic.

The industry has had to overcome several factors inhibiting its growth. As in most European countries, West Germany is desperately trying to correct misdevelopment of the past. Funds directed to programs to keep unemployment low is therefore not available to develop an infrastructure of change and support future-oriented technologies. Moreover, a national market of limited size hampers the introduction and success of new products. And although efforts are being made by European producers to cooperate in a common strategy for new product introduction, such moves are still in their infancy.

With this background, European companies have turned to exports as a necessity for success. This allows them to increase production, employment, and returns. It also means a more aggressive stance when it comes to international competitiveness.

Cover: The Black Forest forms a placid backdrop to high-tech facilities such as Intermetall's Freiberg plant.

Above: The Munich Fairs are a periodic reconfirmation of the German electronics industry's continuing vitality.

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Although export growth rate is falling slightly—especially exports to the U. S.—business with foreign countries is still an important stimulant to the West German economy. It not only increases production and employment, but also the tendency to invest. Exports also maintain a steady increase in income and private consumption—gross national product for 1985 is expected to increase 3% over last year.

While no records are being broken, the state of the semiconductor industry in the Federal Republic of Germany is at least somewhat more satisfactory than in other European countries. Some areas are even doing quite well. For example, Gernot Oswald of Siemens AG Components Division says he is more than satisfied with sales of custom integrated circuits.

The Components Section of the Association of the Electrotechnical Industry expects market growth this year of around 10%, to $3.74 billion. Industrial electronics for electromechanical components takes the biggest share ($327.42 million), followed by active components ($287 million) and passive components ($170 million). In 1984, industrial electronics sold $785.4 million in the internal market—a growth of 27%. This year, sales are expected to increase 24%.

Telecommunications is the second fastest growing area. Hermann R. Franz, president of Siemens Components, predicts that this is one area in which the European semiconductor industry will find good future income. Digitalization of communications networks and their integration in the Integrated Services Digital Network will spur development of integrated circuits as signal processors, peripheral board controllers, ISDN ICs, and the Eurom IC, with more than 130,000 irregular functions on one chip.

Other fields in which Europe could contribute profitably and successfully in the future, says Franz, are automotive electronics and measurement, control and energy technology—with ASICs and power semiconductors—microwave technology and optoelectronics.

Hans Weinerth, Technical Director of Valvo and president of the Microelectronics Committee of the Engineers' Associations VDI/VDE, points out: "We are at the beginning of a ten-year period which will lead the U. S. very close to physical boundaries. On the one hand, this will not cause saturation in the corresponding technology, but financial and engineering efforts must be considerably increased with every innovative step. Intellectual cooperation in West Germany and Europe could oppose competing economic powers like the U. S. and Japan. One contribution is the submicron program of the Ministry of Research and Technology and the Megabit Project in cooperation with Siemens and Philips/Valvo."

A great deal of all technology activities takes place in Bavaria (see page 17E) supported by its minister president Franz Josef Strauss. Other states of West Germany are trying hard to compete: Nordrhein-Westphalia and especially Bavaria's neighbor in the west, Baden-Württemberg (see page 24E)—with a world export share of 1.5%, above that of Switzerland and Sweden. Minister president Lothar Spath spends $1.19 billion per year for science. He encourages innovative industries like information technology, biotechnology, laser technology, and material research to join renowned companies in his state—for example, IBM, Mercedes Benz, and Porsche in the Stuttgart area, ITT Semiconductors in the Black Forest, and numerous machine tool builders from Heidelberg down to Lake Constance.

Most top managers of West German semiconductor producers see early indications for a beginning new boom in the IC business. For 1985, they expect a growth of 10% to 12% (based chiefly on bookings from 1984). Forecasts for 1986 differ widely from 5% to 12%, and some of them suspect a new supply bottleneck in the first quarter of 1986. In any case, the prognosis for 1987 is very optimistic: from a 10% to 30% increase.

A new generation of Bayer plastics

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It is important that ABS plastics maintain good flow properties to guarantee accurate reproduction of the mold detail, ensure perfect mold fill even with low well thickness and long flow paths, and produce immaculate surface quality of the plastics components. Within the new Novodur generation, special emphasis has been attached to these product characteristics. Novodur P2H-AT has the following combination of data: flow length (spiral test) 60 cm (240°C), notched impact strength (Charpy) 11 kJ/m², Vicat-Softening-Temperature VST/B 120 value of 97°C.

Where the toughness of ABS plastics components is the main requirement, attempts are generally made to ensure that the other important properties—such as flow, hardness, and thermal stability—are kept as high as possible. This principle has been achieved particularly well with the new Novodur generation, e.g. with the type P2M-AT, which is important for injection molding.

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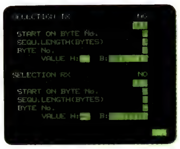

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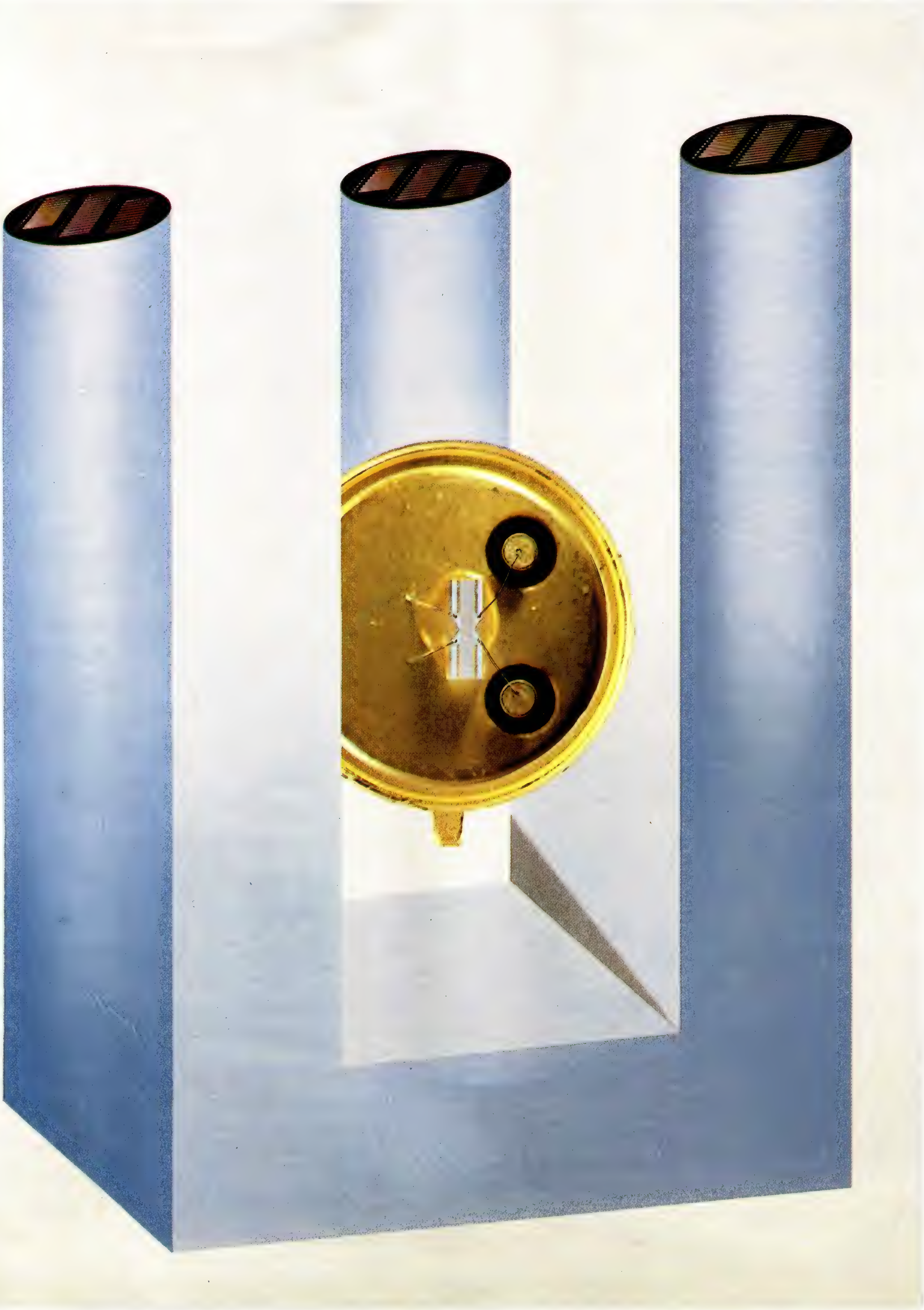

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It has been possible, through the use of improved additive systems, to considerably extend the field of application of the new Novodur generation. For instance, a number of fire-retarded Novodur types have been developed which are geared to the specific needs of the television, office equipment, data processing, and computer industries.

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Toshiba Corp. has developed a 1-megabit C-MOS dynamic random access memory. Ideal as a data storage device, the company sees its primary use in a wide range of computers, office equipment, and portable electronic equipment because of its large memory capacity, high speed, and low power consumption.

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Jermyn signs distribution pacts with SGS and Thomson

Jermyn GmbH, headquartered in Bad Camberg, West Germany, has significantly extended its product offering with the closing of two major distribution contracts with European companies.

Last Spring, the distributor signed with SGS-Ates, Milan, to sell the Italian company's complete line. Jermyn now offers an extensive product range that includes discrete semiconductors, gate arrays, linear integrated circuits, MOS and bipolar integrated circuits, digital logic chips, microcomputers, microprocessors and peripherals, and memories.

To complement this line, Jermyn concluded a distribution contract with Thomson-CSF Bauelemente GmbH for distribution of a wide range of semiconductor products. These include discrete components for power electronic applications as well as Zener and voltage protection diodes, bipolar integrated circuits, driver standard circuits, microprocessors and memories, C-MOS ICs, single chip microcomputers, processors and pheripheral devices of the 9400, 6800, and 68000 families, graphic display processors, telecom ICs, and memories. Also included in the deal are gate arrays in MOS and bipolar technology.

Deal. Jermyn's Hans Peter Friedrich, Pietro Fox of SGS jointly agree on distribution.

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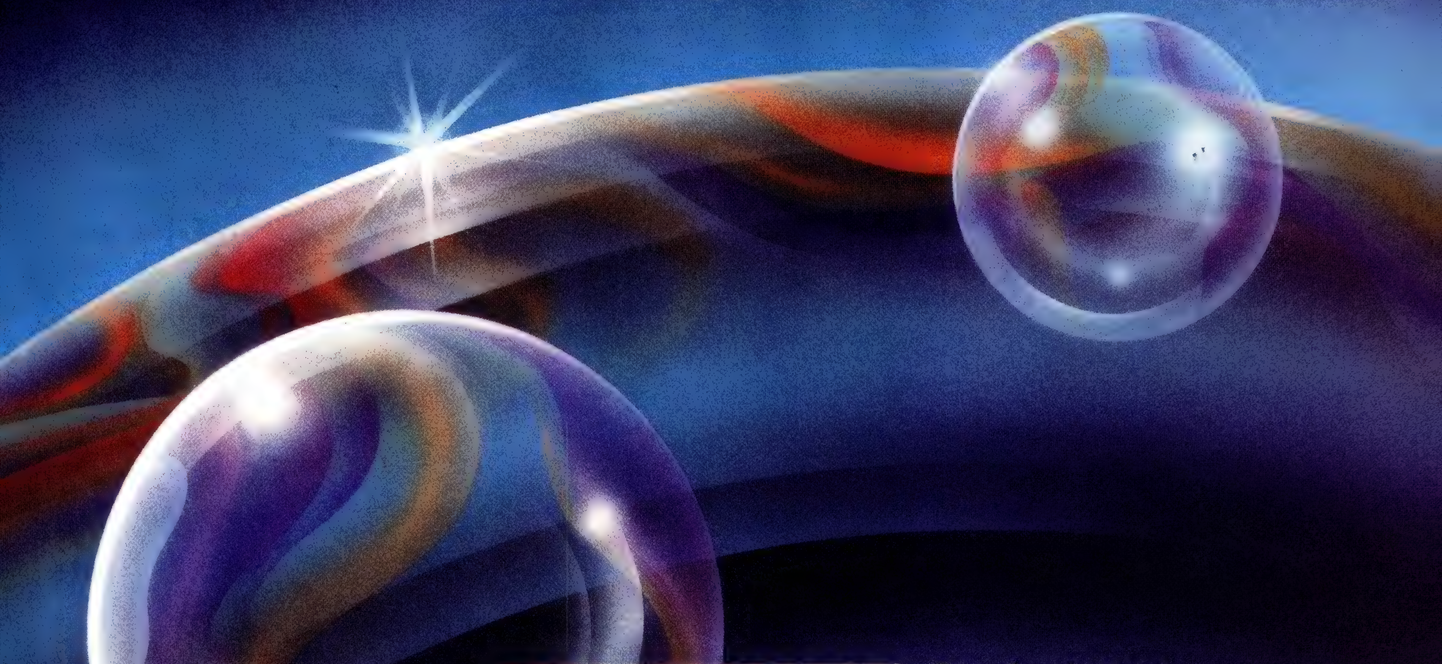

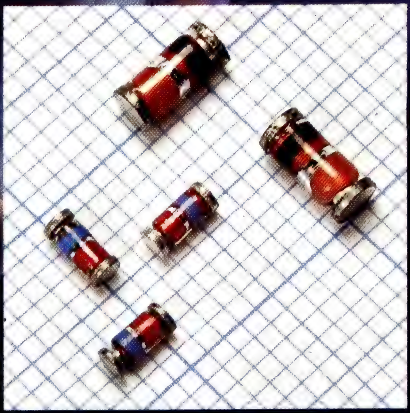

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Mitsubishi continues high growth

Mitsubishi Electric Europe GmbH expects another growth year in 1985, with sales up 25% over last year. Revenue from electrical components are expected to grow by 60%.

In semiconductors, Mitsubishi is an international leader in the electronics industry and employs the world's most sophisticated technology in creating random-access memories, erasable programmable read-only memories, gallium arsenide field-effect transistors for satellite communications, and linear integrated circuits for optical, video, and audio equipment. Although it has a flawless reputation for quality and precision, Mitsubishi is striving to make improvements in the areas of technology and product quality.

In all of this, Mitsubishi is determined to continue its production of ICs and large-scale integrated devices to enhance society in many different ways. Research and development laboratories ensure that the company maintains its leading edge in electronics technology.

Mitsubishi has a broad program on floppy disk drives—which is adjusted to the needs of the European customers—mainly concentrated on half-height 3.5-, 5.25-, and 8-in. drives. Storage capacities range from 0.5 megabytes to 20 megabytes. Also available are Winchester disk drives, 5.25-in. models holding up to 13 megabytes and 8-in. versions holding as much as 250 megabytes.

As a pioneer, Mitsubishi provides color cathode-ray-tube display monitors with low, medium, high, and ultrahigh resolutions; a wide range of CRT sizes, horizontal frequencies from 15 to 110 kilohertz. It provides such options as long persistence phospher, antiglare screens, and super-high contrast for diverse applications. The corporation also leads in monochrome technology, exhibited in its line of clear, crisp CRT and TV monitors.

Moreover, Mitsubishi provides many types of thermal heads to meet various needs, employing both thick and thin film technologies, with a wide range of printing width and resolutions from 3 to 16 dots/mm.

The European headquarters of this traditional Japanese enterprise has constructed a new building in Ratingen near Düsseldorf and moved into it this year. Experience from tradition, combined with the claim of being "the first among many" is the maxim of Mitsubishi's corporate policy.

alphabet character is memorized by using 8 bits of information). This is four times that of a 256-K DRAM chip. In support of Toshiba's new chip, research and development on both N-MOS and C-MOS versions is being carried out by semiconductor manufacturers around the world.

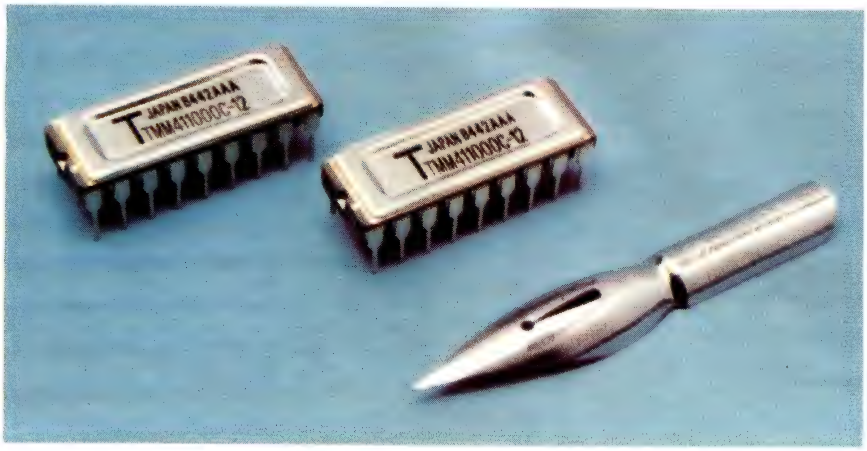
The new 1-Mb C-MOS chip operates at higher speed (about 1.5 times) using less power (about .75%) than a standard 256-K N-MOS DRAM chip currently on the market.

In addition, the new chip has an improved rate of "soft error"—unexpected change of stored information caused by alpha particles from the package to the chip—compared to a 256-K chip.

Operated by a 5-V single power source, the new Toshiba DRAM chip has an access time of 60 ns, the world's fastest for a 1-Mb chip. Power consumption has been limited to as low as 30 mA during stand-by. Moreover, it incorporates a static column mode function that makes possible an access time of 25 ns.

The new device integrates approximately 2.2 million elements on a 5 mm x 12.5 mm chip. Various technologies that made possible the high level integration include: 1.2 um n-well C-MOS process to form a circuit; high performance reactive ion etching oxide film, polysilicon and aluminum; reliable thin film formation in order to increase capacitance of a condensor; and a high breakdown voltage transistor.

Toshiba started the world's first sample shipments of these devices to major computer and office automation manufacturers in Japan and abroad in June 1985. Toshiba also recently announced that the mass production of the 1-Mb DRAM will begin as early spring 1986. The initial production volume will amount to 100,000 pieces per month.



Powerhouse. Toshiba's new 1-megabit DRAM chip, operated by a 5-V single power source, has an access time of 60 ns, the world's fastest. Samples began shipping last June, with full production of 100,000 units a month expected next Spring.

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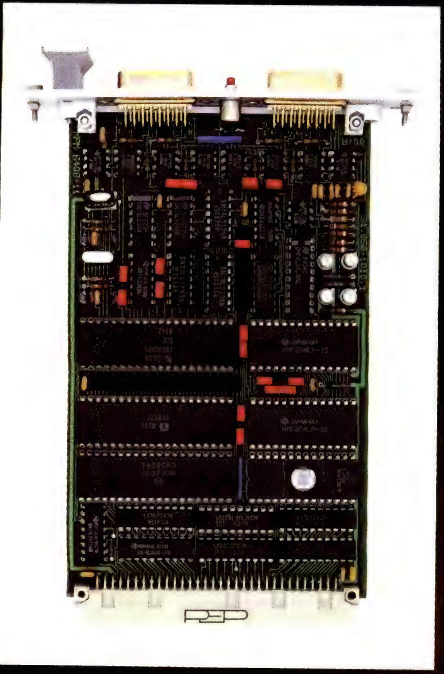

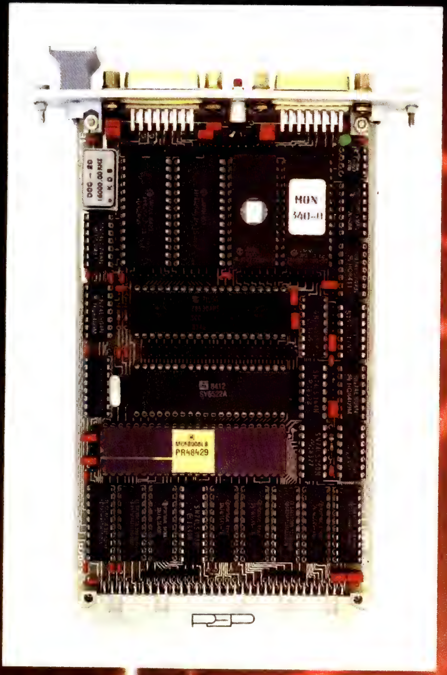

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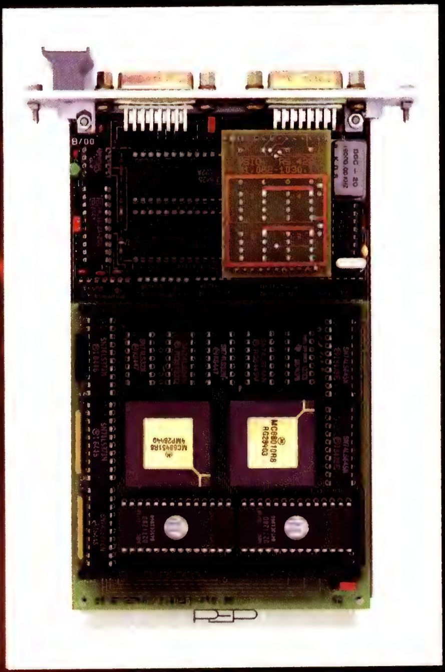

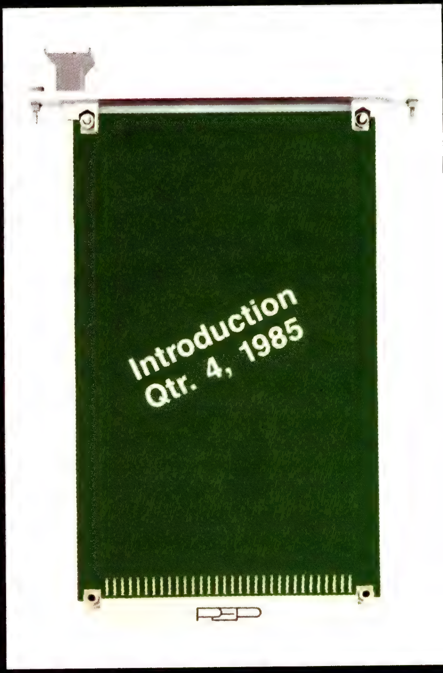

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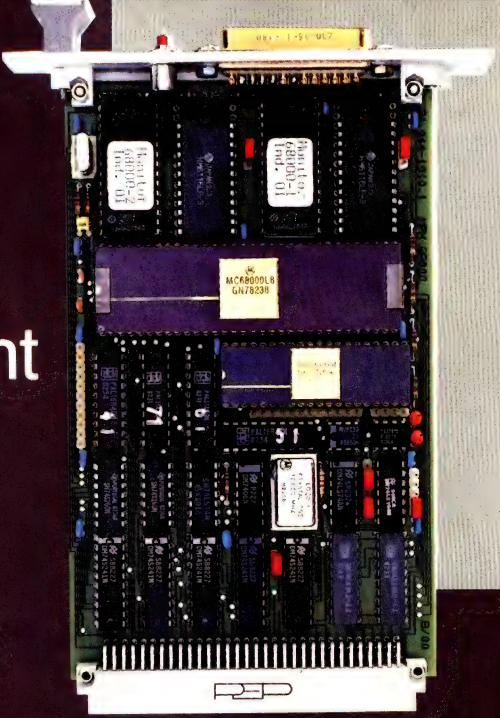

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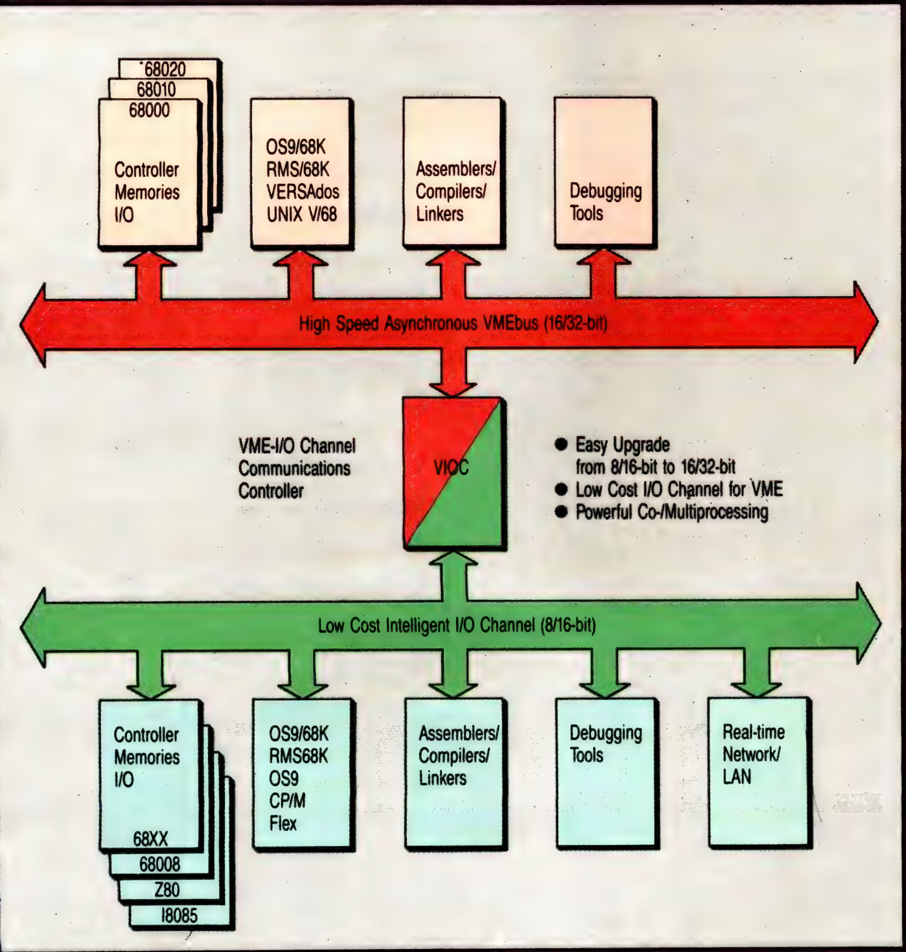

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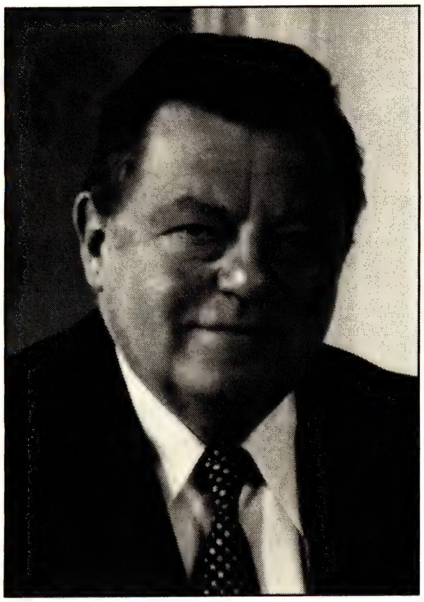
BAVARIA—A technological future

by Minister President Franz Joseph Strauss



Without scientific and technical progress there can be no life worth living and no future with hope. Therefore, we must exploit, with reason and sense of responsibility, the opportunities that science and technology have given us.

In the state of Bavaria, these opportunities were recognized long ago. A region devoid of raw materials can face up to international competition only if the resource "human intelligence" is tapped to develop modern fabrication techniques and "intelligent" products.

Bavaria has strongly advocated a policy aimed at establishing modern and ecologically clean industries with growth potential. Thus, the state has become a preferred economic center in West Germany.

Nearly half of Germany's aerospace industry settled in Bavaria after the war. One out of four jobs in electronics is in Bavaria. Export figures, too, testify to the State's top position in technical fields.

Of total production, almost 30% is exported. Significantly, the electrical/electronics, machine-building, and automobile sectors account for more than half of total exports. Little wonder that Bavaria's industry has become a desirable partner in international cooperation in business and technology. A good example is the substantial share that the state's industry had in the development of the European Airbus.

The strongest push in innovation is presently taking place in microelectronics. Highly integrated microelectronic components are determining the direction that communications and information technology is taking. The ongoing efforts to drive microelectronics sophistication to ever-higher levels are as vital to communications and computer technology as they are to the advancement of new electronics media such as cable TV and videotex.

Meanwhile, microchip production has given jobs to more than 10,000 people in Bavaria. The state accounts for 40% of West Germany's semiconductor production. Bavaria has thus carved out an excellent position for itself. In microelectronics, it will remain a center for technical progress in the future as well.

With their magnetically levitated train, Transrapid, Bavarian firms have developed the means of transportation for the future. In the aerospace industry, Bavarian firms enjoy an excellent reputation. Communication satellites, solar generators for powering vehicles in space, as well as participation in the U. S. space shuttle program are just a few examples illustrating that Bavarian is on the right track in the aerospace sector.

Pursuing judicious, forward-looking and measured policies, Bavaria has created the basis upon which the state's economic power and well-being can be maintained and even expanded. For all the aspirations to economic success and technical progress, however, one should keep in mind that Bavaria's attraction also rests, in no small measure, on the region's culture and natural beauty.

VMEbus and IIOC modules

Through powerful I6/32-bit microprocessors and high density memory chips, it is now possible to achieve minicomputer power with microcomputers implemented with single-height or double-height Eurocards.

Complete single board computers with a 68000 central processing unit, parallel input-output, serial I/O, timers, interrupt controller and random-access memory/read-only memory or, as another example, 1-megabyte DRAM with byte parity are already possible on a single height module for the asynchronous VMEbus.

Both formats use the standardized P1 connector for the VMEbus and VMSbus. The P2 connector, which is reserved for 32-bit VMEbus extension as well as for the local VMXbus, is also used for the I/O channel on double height modules.

Some of the double height modules on the market are also using parts of the VMXbus for the I/O channel. Those modules cannot be mixed with modules using the same VMXbus as local bus for CPU, memory, and DMA devices. Single height modules do not occupy P2 for the I/O, and will allow easy 32-bit and VMXbus extension through a front-ended P2 connector in the future. It should also be possible to have 1 megabyte of local memory already on the CPU module together with the MC68020 CPU and a PMMUuMC6885 and/or a floating point MC68881.

PEP Modular Computers offers a broad range of modules for the

VMEbus as well as for an 8-bit Intelligent I/O Channel (IIOC) in a common single height format of 4 x 6¼ in. (100 x 160 mm). Technological trends support the smaller format with the availability of more and more complex functions integrated in single chips, such as pheripheral controllers or complete bus interfaces. Future packaging techniques such as surface mounting also support the smaller modules. There are also some economic aspects which should be considered when one or the other format is chosen.

Lower cost. With single height modules, it is less expensive to tailor a modular system to a dedicated application as there are fewer functions implemented on each module, resulting in a minimum of overhead functions. Because there are fewer functions, there are fewer components on a single height module; power consumption and heat dissipation, as well as the probability of a failure of a module, are reduced. These factors together have a positive influence on the MTBF values of such modules.

Typical MTBF for single height modules are between 40,000 and 50,000 hours, whereas values for double height modules range between 8,000 and 20,000 hours or even below. Due to their small size, single height modules show extremely good mechanical stability and resistance against shock and vibrations.

All single height modules for the VMEbus may be mixed with double height modules, both using the same standardized P1 connector for the VMEbus interface. The I/O connectors on the single height modules are on the front for easy access by users. Using single height modules allow a maximum of flexiblity at a minimum of space consumption.

I/O channel in single height. Solutions for I/O intensive applications realized on the VMEbus only are quite expensive because of the costly I/O cards. The design of cards for the asynchronous VMEbus with its complex timing requires more time and costs than a comparable I/O card on a 8-bit synchronous I/O channel. I/O operations are usually slow and would reduce the throughput on the VMEbus. Having an I/O channel which allows transparent access from the VMEbus eliminates those disadvantages.

The IIOC from PEP allows a transparent access from the VMEbus and uses also modules in single height Eurocards. Complete systems consisting of a VMEbus and IIOC can be built up in a common single height format.

The IIOC from PEP is more than just an I/O channel. The architecture is based on the Eurobus and allows a local I/O processor. The heart of the PEP concept is a VMEbus-to-IIOC communications controller (VIOC). This is a single-height module which occupies one physical slot (P1) and 64 kilobytes of addressing space anywhere on the VMEbus. It is possible to have more than one VIOC installed in a VME system. Existing VME systems with double height modules may also be expanded with the VIOC.

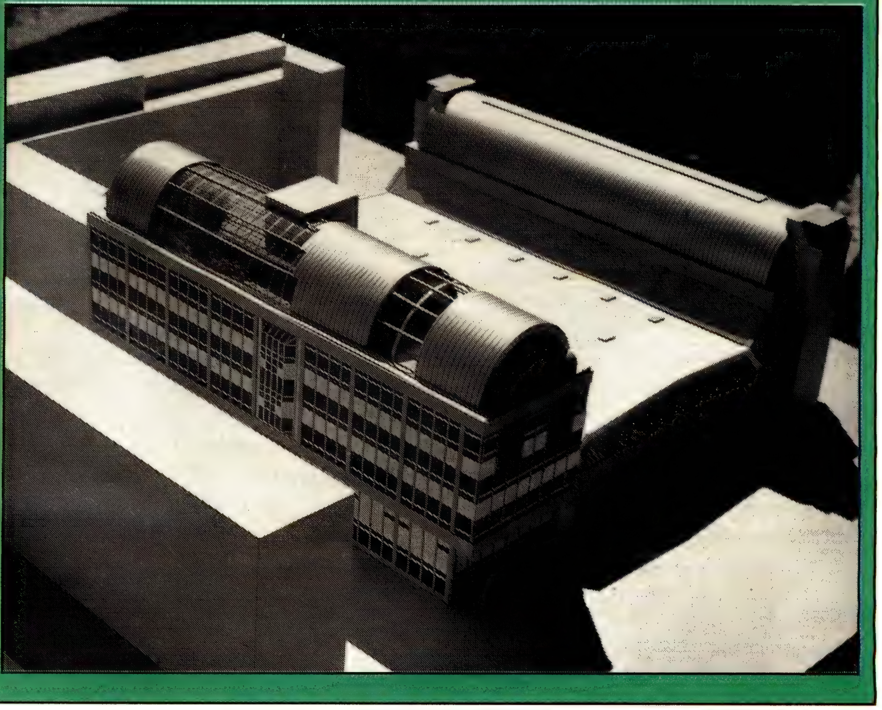
The VIOC module has a flat cable of up to 50 cm length which connects directly to the backplane of the intelligent I/O channel. The VIOC module contains all synchronization

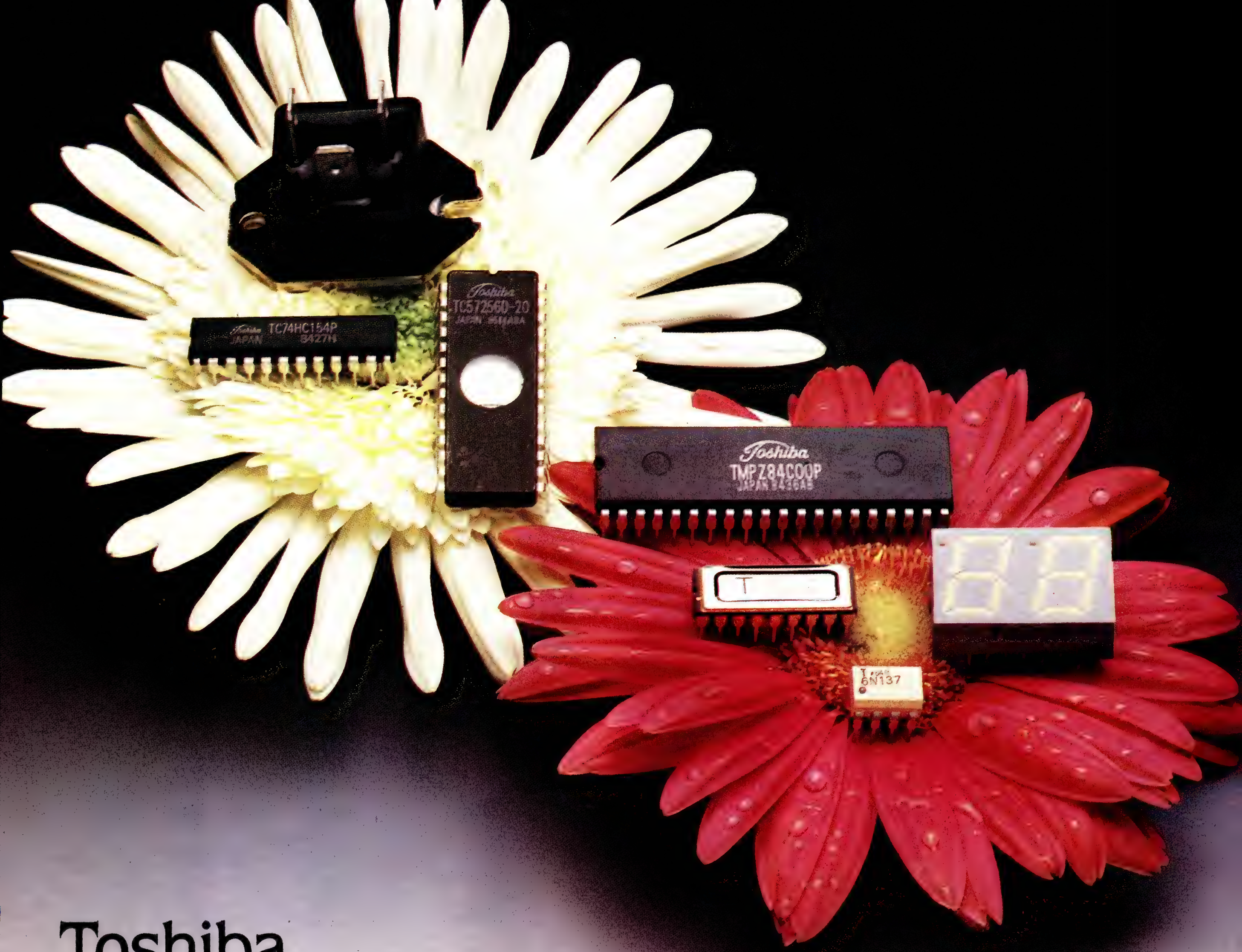
Siemens is a star

The lion's share of business in Bavaria is claimed by Siemens, which concentrates much of its effort in Munich.

Siemens intends to maintain a leadership position in new technologies. In very fast logic, Siemens ranks tops in the world, and for MOS-circuits they are working intensively with Philips and Toshiba on the Megabit Project, which is expected to cost about $578 million. By 1989, Siemens expects to be one of the suppliers of the first 4-megabit chips.

The components division of Siemens had sales of $714 million in the last fiscal year, in addition to $204 million in-house. The world's largest development center (right) has been constructed in Munich's futuristic Satelare industrial park under construction in Regensburg.





Toshiba semiconductors - the pick of the bunch

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logic to allow a CPU on the VMEbus a transparent access to each memory location or peripheral register on the IIOC in a byte- or word-mode. The access time is around 2 us, depending on the type of access, byte, or word. If a word has to be sent to the 8-bit IIOC, it is automatically split into two bytes. If a word has to be read from the IIOC, the first byte is stored in an on-board register for the VIOC and transmitted together with the second byte as one word to the VMEbus. This concept allows the use of broad range of low-cost I/O modules on the IIOC in a way as if they would be on the VMEbus, but eliminating the complex bus interface for each card.

VME systems with low-cost I/O. PEP and other second-source suppliers offer a broad range of low-cost I/O modules for the IIOC, in most cases eliminating high development costs. Development resources can be assigned for dedicated HW- and SW-projects.

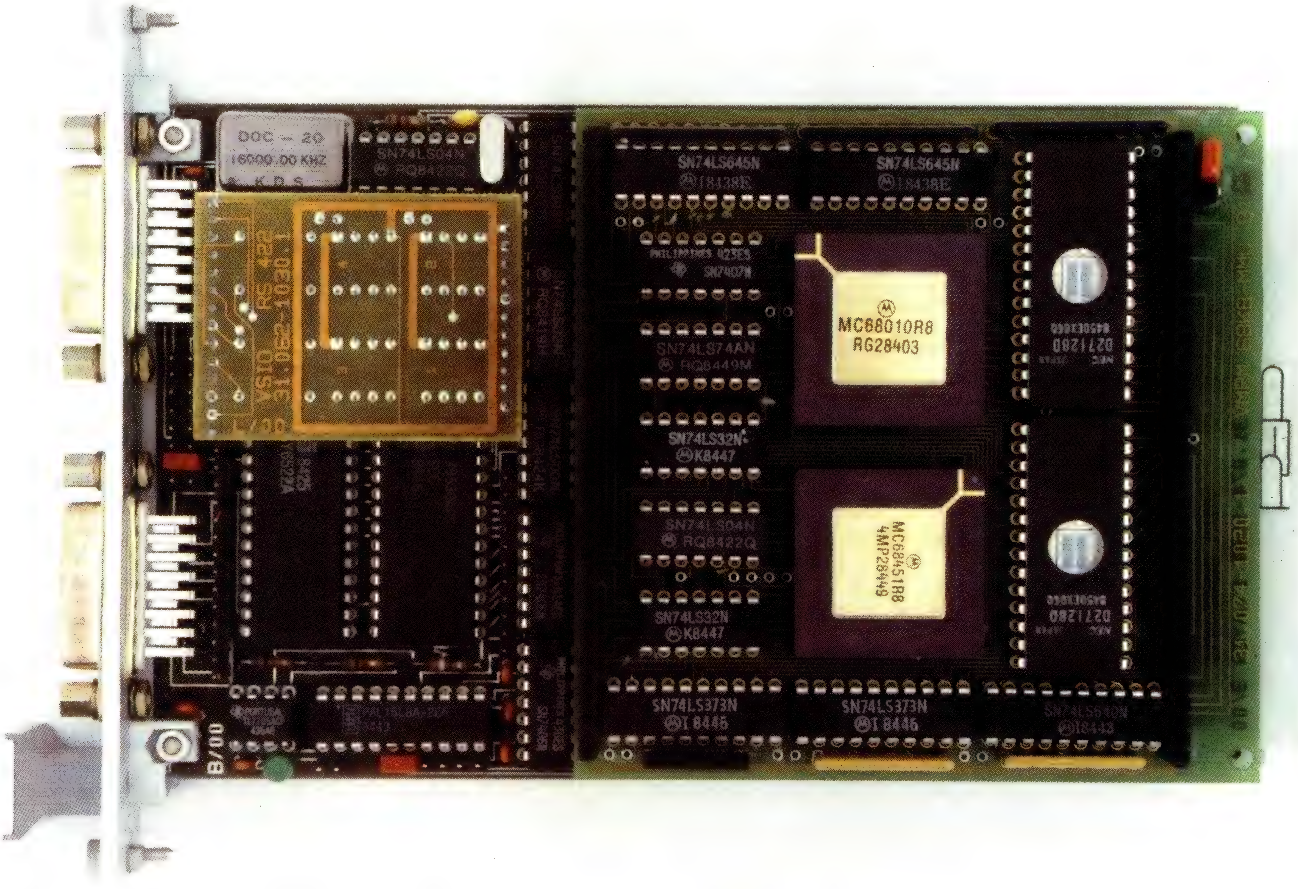
In data acquisition systems or graphic applications, it often is desirable to make some data preprocessing with a 8/16-bit CPU—such as a 68008, 6809, Z80, or I8085—locally on the I/O channel before data is taken over by the master CPU on the VMEbus. The I/O operations and the preprocessing thereby are not occupying the VMEbus. This increases system throughput.

Depending on the application, the CPU on the IIOC may either run an application program in ROMs or run under a ROM-OS, or a disk operating system such as CP/M, Flex, or OS-9, while the VME system runs under OS-9/68K, VERSAdos or another OC.

Both CPUs run simultaneously at full speed only if the CPU on the VMEbus wants to access the IIOC, the VIOC module automatically requests a DMA on the IIOC for each transfer. If there is another DMA controller on the IIOC (i.e., a floppy disk controller) it has higher priority than the VIOC. It is important to know that the master CPU on the VMEbus has access to the IIOC; however, the slave CPU on the I/O channel has no access to the VMEbus. Communications between the CPUs can be implemented by using interrupts or flags indicating a ready condition. Messages and data can be exchanged via a common memory area on the IIOC which is used as a mailbox without the need of dual-ported RAM. Powerful multi- and co-processor systems are possible without the need of complex communications software.

VME system with more than one IIOC. As mentioned above, it is also possible to have more than one IIOC connected to a VMEbus. There is only a physical limitation due to the maximum length of the flat cable between the VIOC module on the VMEbus and the IIOC backpanel. It is also possible to run different operating systems on different I/O channels. Communications between the various I/O channels works then through the master CPU on the VMEbus.

The PEP concept is a cost-effective way of implementing complete VMEbus systems including an I/O channel for applications which require lots of I/O or powerful multi- and co-processing capabilities, all in a compact single



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BADEN-WÜRTTEMBERG: Commitment

by Minister President Lothar Spaeth

Much of what constitutes the state of Baden-Württemberg today was considered Germany's poorhouse during the first half of the last century. The lack of natural wealth (mineral resources are as scarce as energy sources) and the people's dependence on agriculture resulted, during years of poor harvest, in famine and mass emigration.

Today things have changed. Baden-Württemberg is an economically powerful region—it ships 1.5% of total worldwide exports, a share higher than that of Switzerland or Sweden. What makes this even more significant is that Baden-Württemberg's economy is characterized primarily by small and medium-size firms engaged in labor-intensive, metal-processing and finishing activities.

This change in the state's economic structure came about because, beginning with the second half of the last century, politically responsible people faced up to existing economic problems with imagination, perseverence, and level-headedness.

With much the same ingenuity, tenacity, and determination, those engaged in industry, society, and government must take on the challenges of today.

The state government is aware of its responsibility to Baden-Württemberg's future economic well-being, and has made an economic commitment to back up this position. Public expenditures to advance science and technology amount to about $1.9 billion a year. Of this, the universities are to receive roughly $34 million in the 1985/1986 double budget. In addition, research activities at universities will be supported as part of a concentrated-efforts program. For this, the state government has earmarked more than $29 million for 1985 and 1986.

Baden-Württemberg long ago recognized the importance of key technologies such as information technology, bio-technology, laser technology, as well as research into new materials.

All these sectors were also emphasized in the Federal Research Report that the Ministry for Research and Technology issued in May of 1984. In addition to supporting research facilities in the state, aspects of technology transfer are playing an important role.

Intelsat line-up automated

Automation of the highly complicated line-up procedures required by the Intelsat communications satellite has been made feasible by the use of the Satellite Measuring System (SMS) made by Wandel & Goltermann.

The advantages of automated line-up are: a considerable time saving, increased reliability of the measurement, a reduction in manpower requirements in the slave station, and work load decrease of the operator in the master station.

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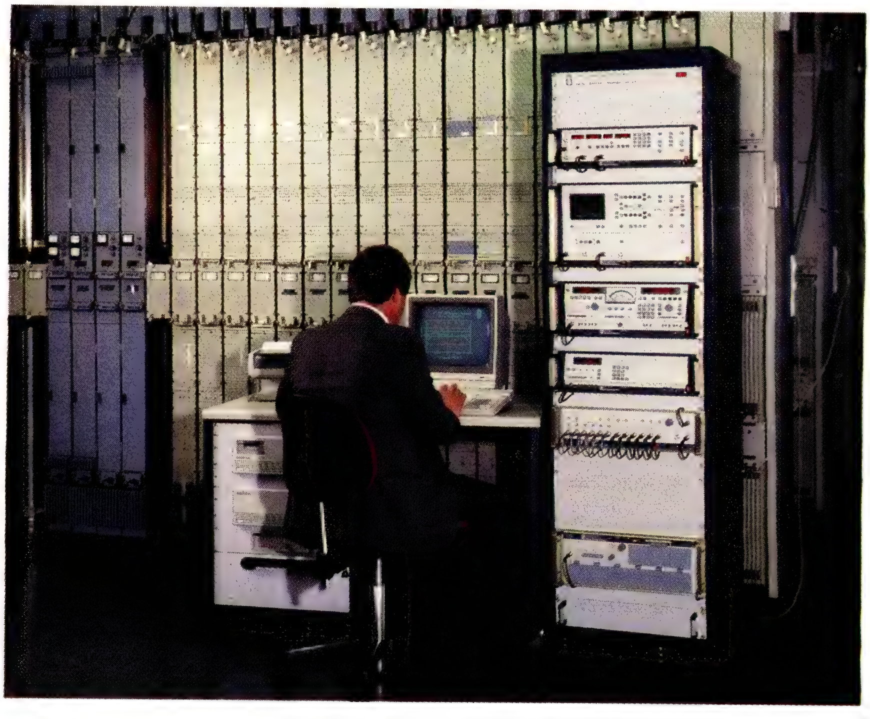

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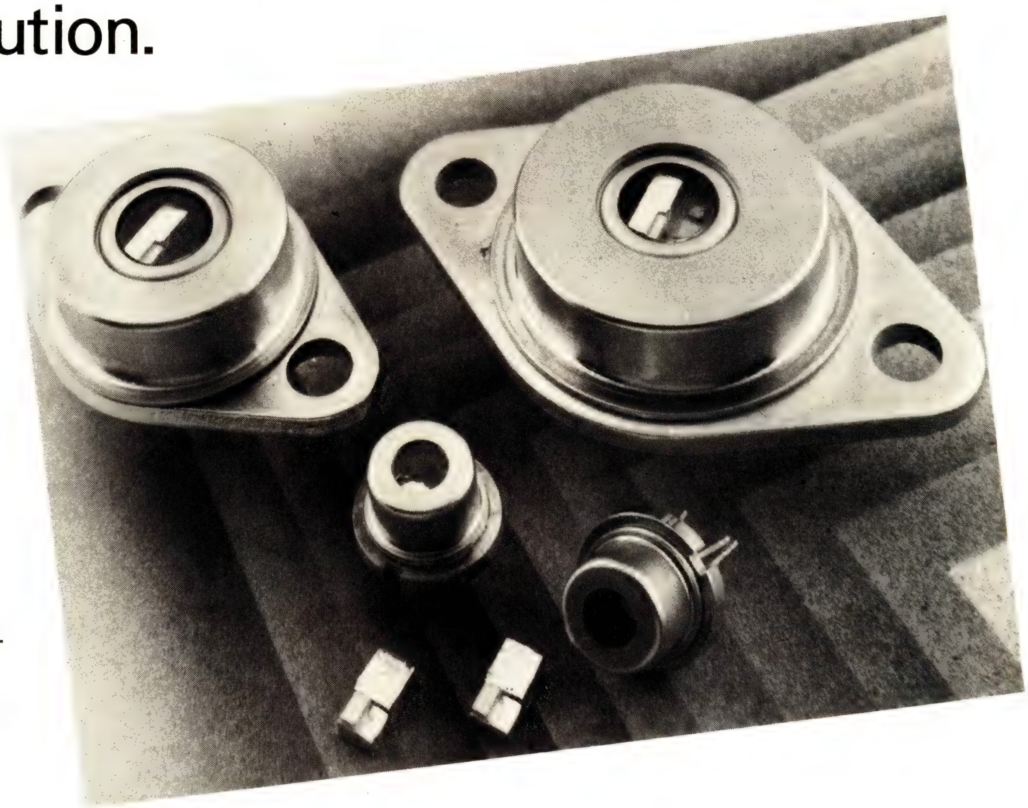

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dialogue is in clear text. Incorrect settings are practically impossible, as they are either carried out automatically following screen dialogue input or—in critical cases—monitor loops (back to back) in the station. An acknowledgment is sent to the master station.

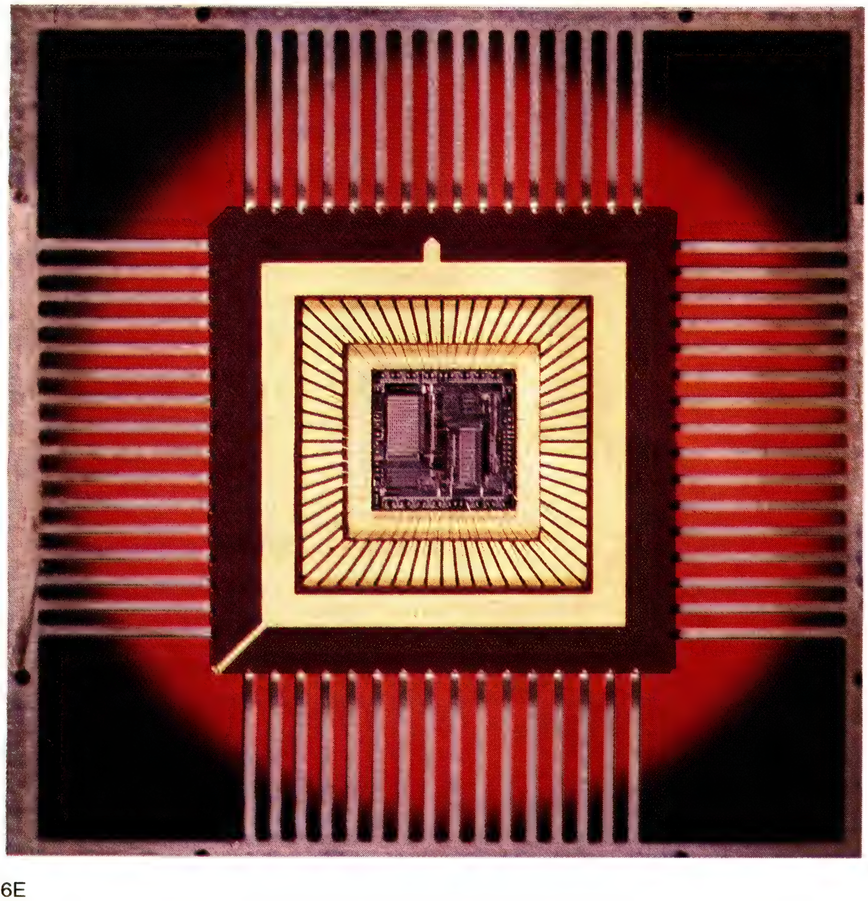
A high degree of reliability is achieved by the many automatic functions. The system allows fully automatic line-up of satellite links to Satellite Systems Operations Guide (SSOG) recommendations in approximately 30 minutes and with protocols in accordance with Intelsat regulations. An automatic control loop in the measuring systems prevents spurious signals from being passed to the transmission system, and automatic correction is provided for cable losses. There is also a complete diagnostic program built in.

The measuring system, which consists of only three instruments in each station, handles all tests between two earth stations. Parameters of all Intelsat systems (12 to 1872 channels) are stored in the database. The computer controls line-up even if a slave station of a same type is not available.

Depending on the measuring task, the SMS outputs result graphically as a table order. All printouts and graphs are in SSOG format. Moreover, all results and parameters are automatically stored on a diskette with sufficient capacity for several complete line-up measurements.

Intermetall—worldwide leadership

It fits in well with the myth and legend of Germany's Black Forest. Located in Freiburg is the locus plant of the far-flung ITT Semiconductor Group. Part of the activities of ITT Industrial Technology Corp., the Semiconductor Group encompasses a worldwide organization employing more than 2,800 people. This includes more than 500 engineers in the development, engineering, and quality assurance departments alone. Manufacturing is done at four plants in Europe (located in France, Germany, and Italy) and two plants in the U. S.



The group, directed by Lubo Micic, is one of the largest semiconductor manufacturers in the world and the biggest manufacturer of silicon diodes. It supplies more than a third of the world's requirements. More than 5 billion discrete semiconductors and over 130 million integrated circuits are manufactured annually—a production of more than 20 million semiconductors a day.

At the Intermetall plant, concept engineering, development, production assembly, measurement, testing, and marketing are concentrated under one roof. One of the group's specialities is the development and manufacturing of discrete semiconductors and ICs, mainly for use in consumer, telecommunication, and automotive electronics. By means of highly automated assembly equipment developed in-house, Intermetall is geared to mass production with a high-quality standard.

ITT Semiconductors has installed at Intermetall's Freiburg plant the most modern wafer fab in Europe for 5-in. wafers and very large-scale integrated circuit technologies. It launched, as early as 1981, the world's first digital real-time signal processing for consumer electronics with its Digit 2000 Digital TV system. This innovation has given new momentum to the entire entertainment electronics industry.

The realization of advanced semiconductors requires not only the very latest technologies but also the very latest manufacturing techniques and the most modern equipment. The highly advanced installations at the Freiburg plant for coating, exposure, plasma etching, ion implantation, diffusion, and oxidation as well as the very latest generation of test and monitoring computers operate under ultraclean condition.

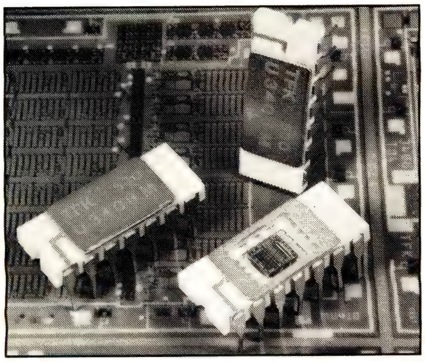
Real-time signal processing for consumer and telecommunication electronics, designed, developed, and produced at Intermetall's plant will thus ensure tomorrow's markets in these increasingly important fields.

With investments of about $23.8 million a year, with an above-average export share to the Far East and U. S., and the concentration on a relatively small product range, the worldwide ITT Semiconductors Group will certainly keep or even increase its leadership position in the world's markets. ☐

Telefunken's Programmable S/C-Filter. Telefunken's single-chip, mask-programmable switched-capacitor filter array, U 3408 M, is designed for audio- and telecommunication applications to replace the complicated electromechanical LC-filter of 8th order.

The filter is fabricated in a n-well double-poly complementary-MOS process. It contains four identical biquad filter sections, one programmable active distributed RC anti-aliasing filter, and two identical uncommitted operational amplifiers, oscillator and programmable frequency divider.

By interconnecting 32 capacitor arrays and 64 analog switches to the op-amps, a variety of filter types and characteristics up



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28 October - 1 November

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6th International Trade Fair for Electronics Production
12 - 16 November

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1st International Trade Fair for Computer Integration in Logistics, Development, Design, Production and Quality Assurance with Congress
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to the 8th order can be realized only by customizing the metal mask as in digital gate arrays.

The filters mounted in DIL plastic or DIL ceramic case are available as custom designs or as standard filter. They require a minimum of external components and no adjustment.

Typical application are in the extended audio range up to 40 KHz with a minimum supply voltage of 5V.

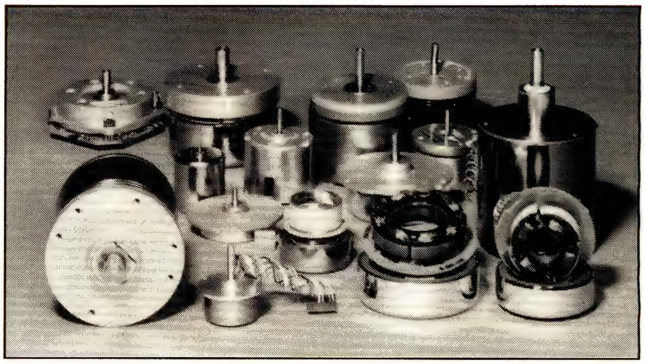
Lithium battery for backup memory. The research and development laboratories of Varta Batterie AG, Hannover, West Germany, have developed a new type of lithium battery targeted for electronic applications. The new batteries grow out of Varta's work in nickel-cadmium secondary cells and alkaline and lithium primary batteries.

Varta's new batteries feature a shelf life of more than 10 years, and one of the highest energy densities of currently available battery systems. This makes these batteries an ideal partner in electronic memory- and real-time clock-back up and comparable applications.

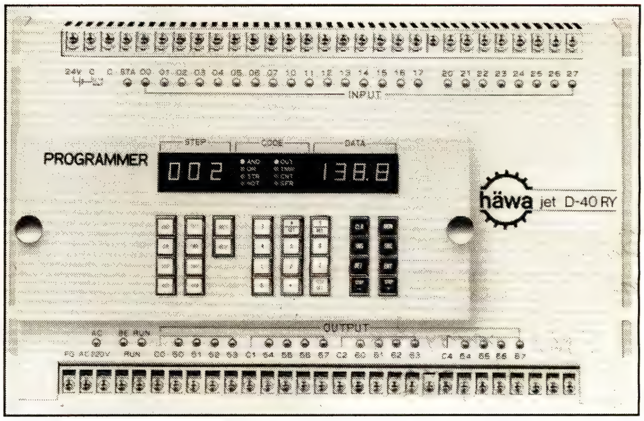
As positive counterpart to the lithium electrode, a bobbin-type chromium-oxide electrode was chosen. The cell has a practical energy density of approximately 1 wh/cm³. With o.c.v. of 3.8 V, the operating voltage is 3 V. The self-discharge rate is below 1% per year at room temperature. Operating temperature ranges from -30°C to +75°C. Under *normal* operating conditions, there is no voltage delay.

A new range of DC motors. Papst-Motoren GmbH has expanded its line of miniature DC motors with a new series of electronically commutated DC motors of external and internal rotor design, and a series of mechanically commuted types with ironless rotor and permanent-magnet exciter.

Papst, which has specialized in precision drive DC motors for use in computer peripherals, office machines, and audio and video technology, has pioneered in electronically commutated motors of single or multiple phase design which employ frictionless rotor-position indicators.



The expanded Papst line includes versions with external circuitry, as well as models employing commutation and control electronics integrated into the motor. Additional design flexibility is achieved with component kits containing the stator, rotor, and electronics. DC motors with mechanical commutation and permanent-magnet exciter adapt easily to complex electronics application. The use of an ironless rotor is of advantage when exacting requirements for speed constancy, switching frequency, and acceleration are imposed.

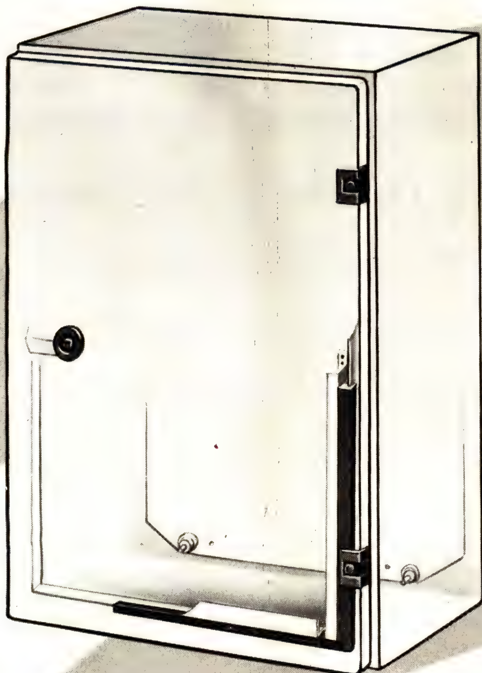


Programmable control systems for plant automation. Versatility is the keyword for a line of programmable control systems for plant automation being introduced by Häwa AG. The jet-sps D-series has been designed to cover a complete range of programs for small- to medium-sized programming applications.

The 4 basic models—D-20, D-28, D-40, and D-64—offer 20 to 64 input/output processing functions and can be expanded up to 128 I/O functions. Each model is offered in three different versions with contact output, SSR output, and transistor output.

The four models of the D-Series have *the* advantage of simple system configuration because they use same system software, so except for the I/O numbers, there is complete programming compatibility. They also boast a scanning speed of 5ms/1kW, a high degree of reliability because of its single board design, large memory capacity, and build-in shift registers.

häwa offers



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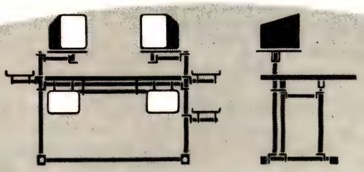
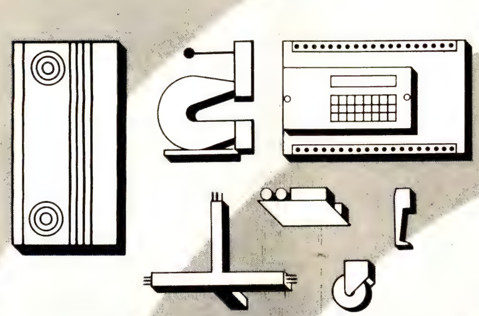


Workstation desks designed with space for system options and a general purpose working area.



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OPTICAL LITHOGRAPHY REFUSES TO DIE

FORECAST TO BE GONE BY NOW, IT MAY LAST FOR THE REST OF CENTURY

by Jerry Lyman

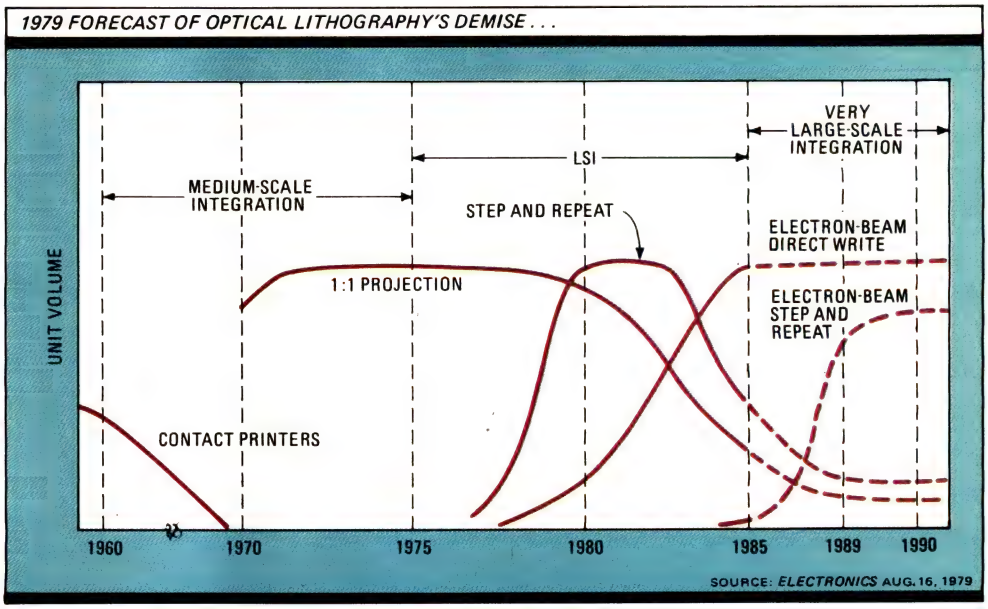
NEW YORK

Like Mark Twain's rumored death, reports of optical lithography's demise have been greatly exaggerated. Predictions in 1979 by the electronics community that this dominant chip-making process would be laid to rest by now and that electron-beam direct-writing systems would dominate the integrated-circuit lithography field turned out to be far off the mark. Optical lithography is thriving in 1985 and will continue to do so well into the next decade.

The reason is simple: optical technology turned out to be a moving target. The process has kept improving without greatly adding to manufacturing costs, eliminating any incentive to move to another technique. "Optical lithography is still the most cost-efficient way to get the job done," says David Elliot, product marketing manager for wafer steppers at GCA Corp. in Burlington, Mass.

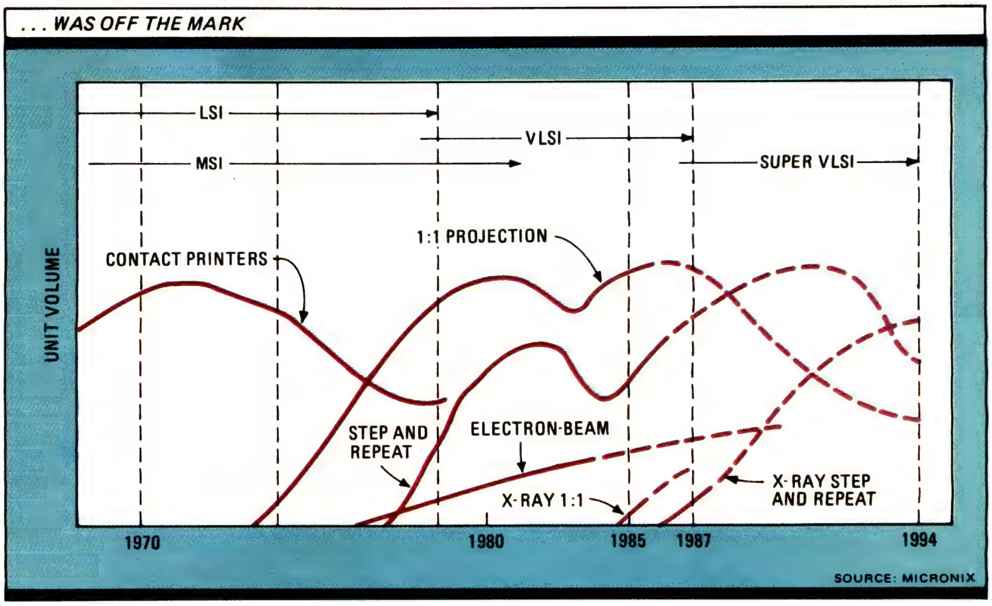
Two factors have enabled optical lithography to dominate the picture. The first is continued improvement in the technology. There are now optical steppers and 1:1 scanning optic systems performing successfully around the 1-μm level. Steppers work by shining a light from an ultraviolet source through an enlarged portion of an IC wafer pattern, known as a reticle. The pattern is projected onto the wafer's resist-covered surface through a reduction lens. After exposure, the machine's table is mechanically stepped to a new site for the next exposure, and this procedure is repeated until the entire wafer is exposed. The reduction stepper eventually will push that figure to as low as 0.5 μm.

1979 FORECAST OF OPTICAL LITHOGRAPHY'S DEMISE . . .



SOURCE: *ELECTRONICS* AUG. 16, 1979

. . . WAS OFF THE MARK



SOURCE: MICRONIX

The scanner, on the other hand, has a complex reflective lens system that uses a mask to project an image the same size as the mask onto a wafer.

The second factor is the failure of the electron-beam technique to carve for itself a position on the IC production floor. Electron-beam's fine-line capability has never been questioned. However, the equipment is difficult to interface with IC production lines because it needs special resists and takes up a lot of space on the floor. In addition, electron-beam systems cost \$3 million to \$4 million, compared with \$700,000 to \$800,000 for optical versions. Adding to the problem: their throughput is low.

As a result, IC-lithography experts

256-K AND 1 Mb DRAM DESIGN FEATURES

Process parameter	256-K DRAM*	1 Mb-DRAM
Die size (sq mils)	52,000	134,000
Overlay accuracy (μm)	0.6	0.4
Device well field-oxide width (μm)	2	1 1/2
Poly II gate width (μm)	2	1 3/4
Buried contact (μm)	1 3/4	1 1/4
Poly III line (μm)	1 1/2	1 1/4
Contact to gate (μm)	1 3/4	1 1/2
Metal (μm)	5 1/4	4

*Based on the Fujitsu MB81256 DRAM.

continue to turn to such optical solutions as the stepper and the 1:1 projection system. GCA and Varian Associates Inc. have decided to terminate their extensive development efforts in electron-beam instruments.

One indication of optical lithography's staying power and adaptibility, as well as the faith that industry experts have in it, is the Department of Defense's recent award to GCA of a four-year, $5 million contract for an optical stepper called the Advanced Wafer Imaging System to be used for producing submicron devices in the Very High-Speed Integrated Circuits program. The 10:1 stepper will be capable of 0.75 μm or better and will be used along with direct-write electron-beam as a production tool for submicron devices.

EXCEPTIONS. IBM Corp. and Fairchild Camera & Instrument Corp. are the exceptions that use direct-writing electron-beam systems to customize the metal layer of partially finished wafers in gate-array applications. Electron-beam systems are being used mainly in mask and reticle production, however, and are likely to stay there for some time.

The next two generations of commercial memory chips—1 and 4 Mb—will be imaged optically. Today's 256-K dynamic random-access memories can be processed with either Perkin-Elmer Corp.'s latest Micralign M600 HT (a 1:1 projection machine) or with any of many optical steppers. The next generation, the 1-Mb DRAM, with its critical levels—such as the 1.25-μm buried contact and three layers of polysilicon lines—will require one of the latest steppers with 1-μm capability or a mix of a 1:1 system and a stepper (see table, above).

Optical technology has improved in a variety of ways since its obituary was written, and it should continue to do so. The major improvements—and the most dramatic—have been in better-resolution lenses and higher numerical apertures, as well as in new and improved photoresist techniques. Also contributing is the increased use of pellicles (transparent reticle protectors) to lessen particle contamination and improve the alignment circuitry. A new laser-scanned reticle printer from Ateq (see page 40) could be a big factor in improved reticle performance, which will aid the optical steppers.

From these have sprung the changes that occurred since 1978 and 1979, when optical lithography was based on 10× steppers and 1:1 scanning projection machines producing mainly 3-μm IC features. Today, the dynamic technology is at the 1.25- to 1-μm level and straining to cross the 1-μm barrier. In fact, optical lithography is already making some submicron circuits in research and development programs.

The DOD is spending $5 million on an optical stepper for VHSIC

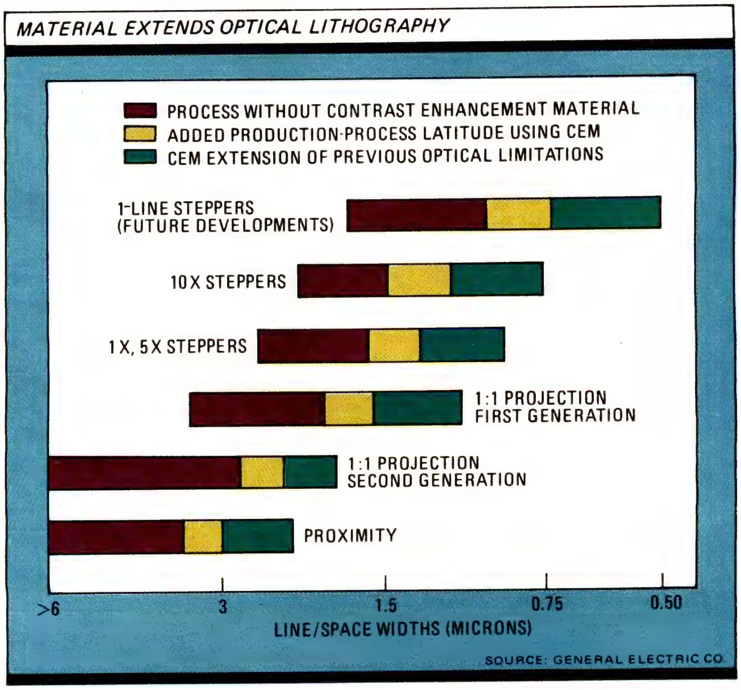
Advances have also been made in illumination sources. For example, today's steppers could theoretically improve dramatically, according to extrapolations, with a deep-ultraviolet lens. Further reductions in wavelength could be achieved using a deep-UV excimer laser source and special fused-quartz lenses. With a hypothetical system of this type, minimum feature sizes of 0.5 to 0.6 μm could possibly be achieved. However, formidable engineering obstacles bar the way to this stage.

Most steppers are still using G (436-nm) and H (405-nm) wavelength light lines as their ultraviolet sources. However, it appears certain that the next generation of steppers will be based on the I-line (365-nm) light sources. That wavelength combined with a high numerical aperture will give a production capability of less than a micron.

Machines of that new breed are already on the market. One is the PAS 2500 5× stepper from ASM Lithography of Tempe, Ariz. It uses a Zeiss I-line lens with a numerical aperture of 0.32 to give a production resolution of 0.91 μm. Still another machine with an I-line lens is the model 804 from TRE Semiconductor Equipment Corp. of Woodland Hills, Calif., which uses a 10:1 Zeiss lens having a numerical aperture of 0.42 giving a production resolution of 0.6 μm.

It is interesting to note that Ultratech Stepper, a division of General Signal in Tempe, Ariz., has introduced a 1-μm lens for its model 1000 wide-field 1:1 stepper. This lens differs in that it is a wideband model, with a numerical aperture of 0.315 that can expose 0.8 μm lines in research applications.

Besides shorter wavelength optical systems, IC processors have explored multilayer resist systems to get the even finer lines required by very large-scale-integration applications such as the VHSIC program. Finer lines require thinner resist coatings, and these coatings are fragile. If a thin resist is spun over a nonplanar surface, the resist will be distributed unevenly over the wafer. This results in a distorted exposure image. Because of this, two- and three-layer resist approaches have been devel-


MATERIAL EXTENDS OPTICAL LITHOGRAPHY

SOURCE: GENERAL ELECTRIC CO.

oped to planarize a wafer's surface and handle efficiently a thin photoresist layer [*Electronics*, June 19, 1980, p. 124].

However, none of the multilevel resist techniques has proven to be processworthy in large-scale production. The problem is that although the techniques work well, they add many steps to the IC-processing flow and therefore are not cost effective.

One possible way out—a new contrast enhancement material (CEM)—was first reported in September 1982 by General Electric Co.'s Corporate Research and Development Laboratories in Schenectady, N. Y. This material is an initially opaque substance that is deposited on top of a photoresist layer. It bleaches to a transparent layer when exposed but remains dark in unexposed regions, thus forming an optical mask. It significantly improves resolution, focus, and exposure latitude, or width, without the number of process steps and the expense required of a multilevel resist (see chart, bottom of p. 37). The new material is in full production and is commercially available. It is already being used by some IC manufacturers. In one case, a gallium arsenide-IC foundry wa able to image 0.35-μm lines using a TRE 10 : 1 stepper with an I-line lens that was enhanced by the GE material.

Electron-beam systems are expensive and space hungry

THE LIMIT. The question now before the industry is where all this activity will lead and whether there is a theoretical or practical limit. John Bruning, vice president and general manager of GCA's Tropel lens-making division in Fairport, N. Y., sees the 5× lens dominating the stepper field. He says most lenses are now being made for the G-line with the next generation of steppers at I-line (a few are already there). Ultimately, he forecasts, the final generation of steppers will have a deep-UV source (perhaps an excimer laser) and quartz optics.

According to a survey by Ruddell and Associates of Trinity Center, Calif., a consulting engineering company and technical market forecaster that tracks the semiconductor-production-equipment industry, in the next few years, the 5 : 1 optical stepper will garner the largest market share from its main competitors, the 10 : 1 stepper (already almost 90% of reduction steppers are 5 : 1), the 1 : 1 stepper, and the 1 : 1 full-projection system. A few of the companies queried in the survey expect the eventual optical limit to be 0.75 μm, but many of them forecast a line width of 0.5 μm.

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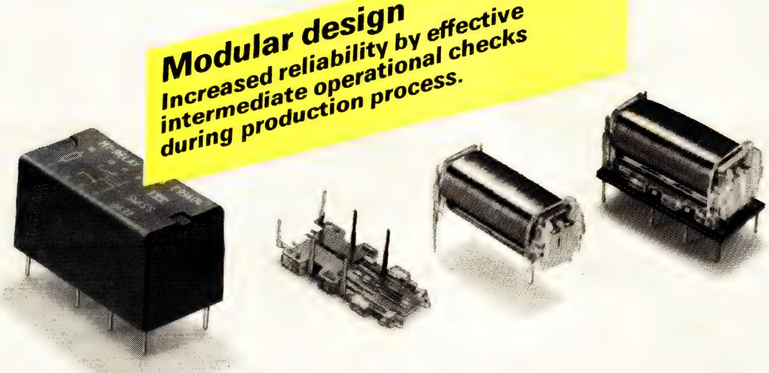

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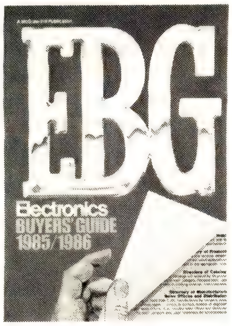

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Their optimism may be well founded. However, such a forecast depends on two things: resolution of half a micron will require better than a tenth of a micron alignment capability (most machines now are at 0.25 to 0.3 μm), and the cleanliness requirements will be extremely tight.

WHAT COMES NEXT. Even with the extended life of optical lithography, and the fact that most experts now see the technique extending well into the 1990s and perhaps to the end of the decade, there still is the question of what comes next. Both X-ray and electron-beam direct writing have their backers. For example, Rick Ruddell, president of Ruddell Associates, sees X-ray lithography, probably in the form of an X-ray stepper in 1987, emerging into the production arena. Aubrey Tobey, vice president of sales at Micronix Inc. of Los Gatos, Calif., also sees X-ray lithography making its entrance at that time.

X-ray technology has advantages over electron-beam direct writing. These include simplicity, absence of proximity effects, large depth of focus, and most important, an immunity to dust. But electron-beam technology has built up a tremendous backlog of design and operational experience, while many design problems remain for X-ray methods. And electron-beam could be a sleeper: until now, most commercial electron-beam efforts have gone for mask making. Only now are the few electron-beam-equipment companies left beginning to concentrate on direct writing.

Perkin-Elmer Corp., Norwalk, Conn., is among the few U. S. companies involved with the three technologies—optical, electron-beam, and X-ray lithography. David Huchital, the company's vice president and general manager, points out that the IC industry's swing to application-specific ICs bodes well for the electron-beam system. That is because those semicustom chips do not require large production volumes; it is cost effective to do them with a direct-writing electron-beam machine rather than producing an expensive and time-intensive reticle for an optical stepper.

Experts say X-ray steppers will be in use by 1987

Despite the 1979 forecasting errors, it would not be farfetched to expect such dark-horse technologies as ion-beam lithography, holography, or even some entirely new method to eventually challenge or replace optical lithography. Or optical lithography might yet continue to confound the experts and retain its dominating position. ☐

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LASER BEAMS SPEED UP RETICLE WRITING

OPTICAL LITHOGRAPHY SYSTEM OUTPERFORMS E-BEAM MASK MAKERS

TECHNOLOGY TO WATCH is a regular feature of *Electronics* that provides readers with exclusive, in-depth reports from companies around the world on important new technical innovations. It covers significant technology, processes, or developments incorporated in major new products. The reports also analyze technical data so that readers can assess the impact of new developments. Neil Burglund, Ateq Corp.'s president, and Paul Warkentin, engineering manager, led development of the Core 2000 reticle generator. Miles Chesney led a team of six cofounders of Meiko Ltd. in the design of the Computing Surface, the subject of the article beginning on p. 43.

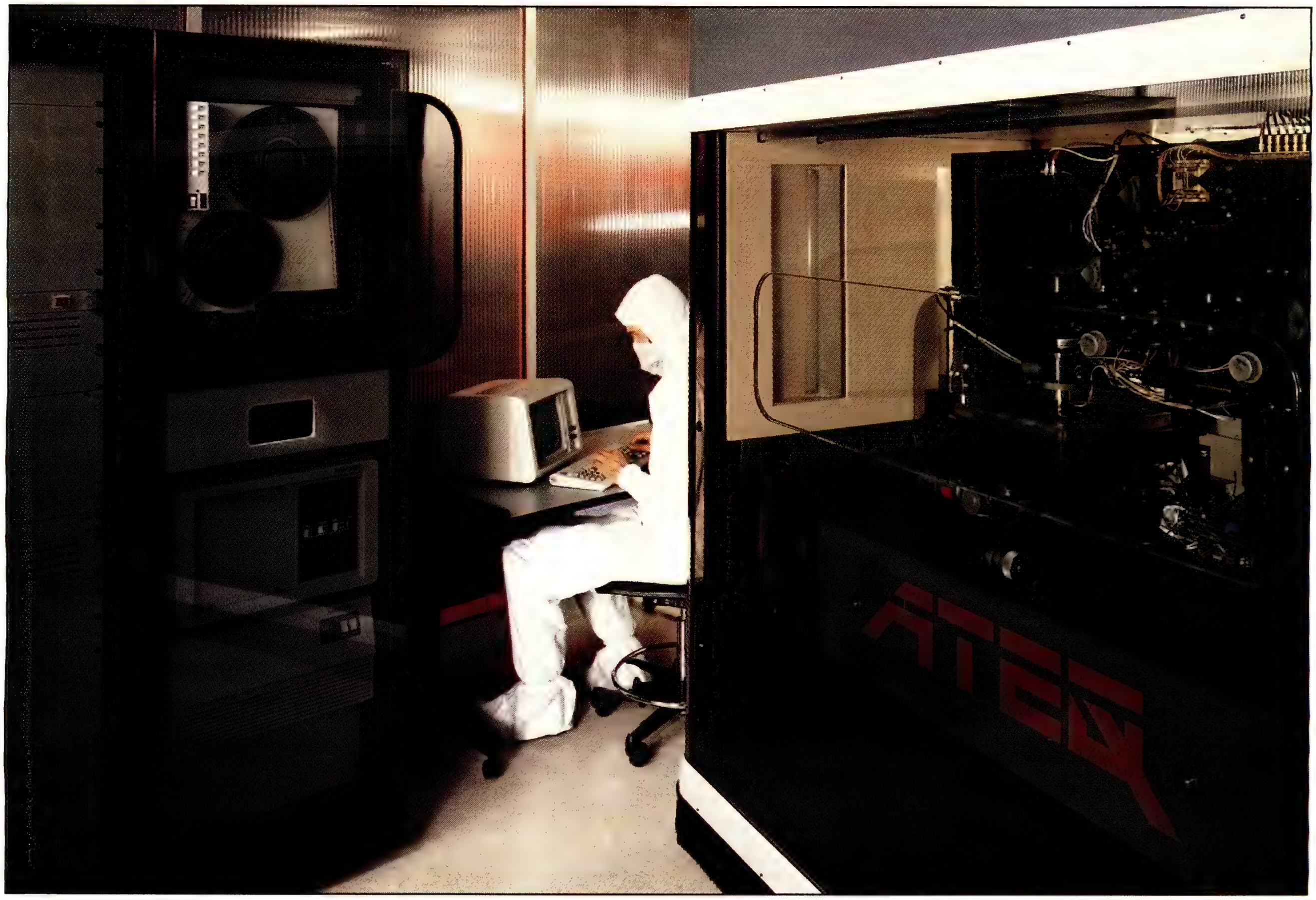
Computer-aided design and engineering may work wonders in increasing the number and quality of very large-scale-integration designs. But on the way to production, these designs run into a bottleneck in the microlithography department. Custom and semicustom layouts must be supported with reticles—precision chrome-on-quartz substrates patterned with integrated-circuit features and used in the lithographic process—and market pressures require rapid turnaround of that time-consuming process for semiconductor vendors to stay competitive.

Ateq Corp.'s Core 2000 is a new kind of reticle generator that provides an easy-to-use alternative to conventional systems with a throughput up to 10 times faster. The reticle writer can easily fit and be compatible with current optical lithography facilities and processes.

The three-year-old Beaverton, Ore., company claims the Core 2000 costs less than existing optical and electron-beam reticle makers, yet outperforms those systems. It combines four proven technologies—laser scanning, raster graphics, precision mechanics, and optics. Despite its highly innovative approach to complex microlithography, the system does not use expensive or incompatible new technologies.

The Ateq Core 2000 (Fig. 1) is a scanned-laser printer in which eight independent parallel laser beams, called a laser brush, expose or print IC patterns by sweeping across the resist covering of a chrome-coated glass or quartz rectangular plate. The system consists of two separate assemblies. One holds the laser, optics, positioning mechanisms, and mask-blank-handling equipment; the other holds the system electronics.

Eight parallel beams created from a single ultraviolet laser are first acousto-optically modulated and then swept across the image plane by a high-speed rotating polygonal mirror (Fig. 2). A precision X-Y table moves at right angles to the swept beams, creating a raster image upon the reticle. A



1. RETICLE WRITER. Ateq's Core 2000 is a reticle-writing system based on laser-scan technology, complex optics, and high-speed circuitry.

steering mirror and modulation timing provide fine control of the beam position.

Most IC companies have settled on optical step-and-repeat systems as the best way to put VLSI circuit patterns on wafers because these systems are cheaper and faster than their electron-beam competition. But generating the necessary reticles to expose the pattern onto the wafer is a slow and expensive step, particularly with the accuracy, throughput, and low defect level needed for chips designed with 1-μm or smaller features.

"With the advent of CAE, the design cycle is no longer the culprit," says Neil Berglund, president of Ateq. "New designs will increase pressure for faster design-to-chip cycles, lower costs, and smaller geometries, which will require even more precise capabilities for reticle making."

The new scanned-laser reticle writer has significant advantages over available equipment based on either optical or electron-beam technology. These include:

- Throughput 5 to 10 times faster than electron-beam methods.
- Higher yield of reticles than is possible with electron-beam technology.
- A footprint one third the size of competitive machines.
- Process compatibility with optical photo resists and electron-beam tape formats.
- Equipment costs that are less than one half those for electron-beam lithography equipment.

The key technical problems in reticle generation are the demands for extremely high precision and information density. Circuit geometries must be written with a position accuracy on the order of one part per million—a proportion comparable to the width of a human hair against that of a football field.

When treated as a digital raster image, the reticle requires more than 60 billion pixels. For a 5-in. reticle, this is equivalent to 10,000 TV images per square inch. A single reticle holds the equivalent of 250,000 frames of video, or about three hours of viewing.

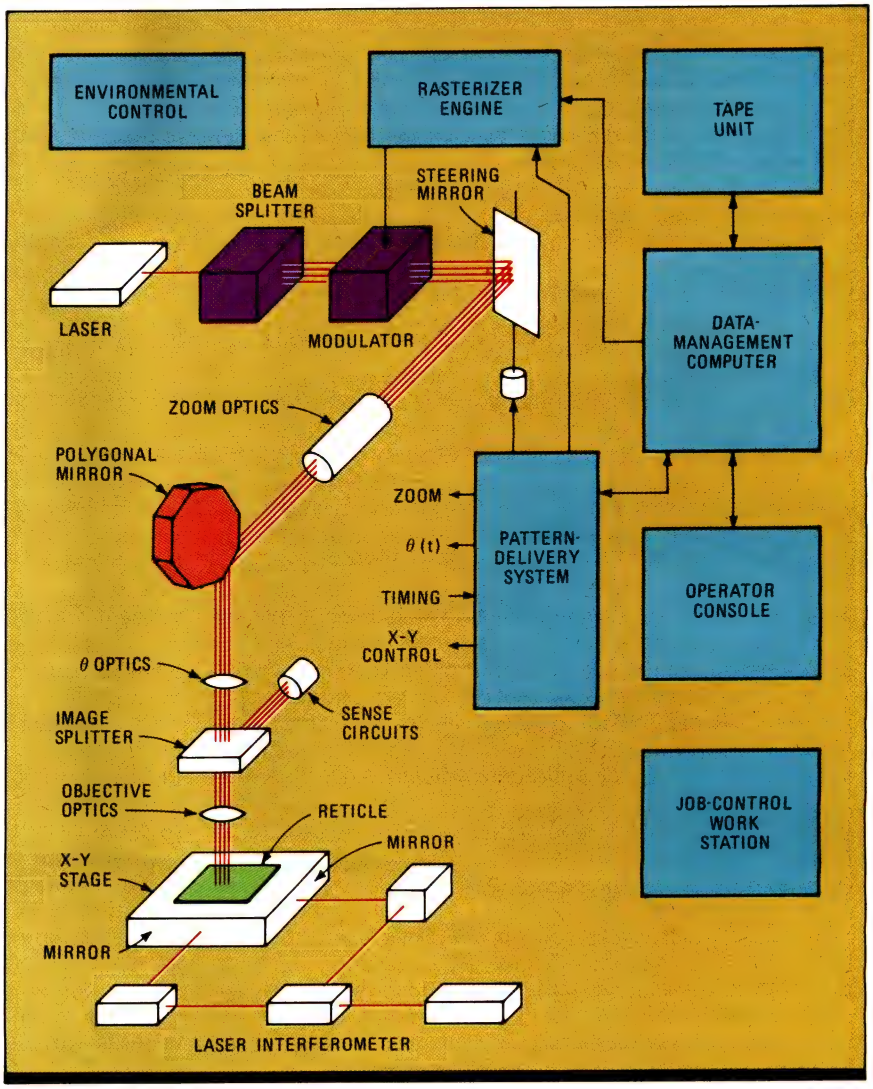
Ateq's scan-laser reticle generator has several advantages over optical-pattern generators and electron-beam lithography systems. Optical-pattern generation, although an established technique, is falling behind in its abilities to handle VLSI. Optical capabilities have become very sophisticated and image quality is unsurpassed, but the mechanical apertures of pattern-generation equipment are effective only up to levels of 10,000 devices on a chip—roughly equivalent to a 1-K random-access memory. On circuits any denser than this, throughput is too slow.

Electron-beam technology was developed originally for direct writing on silicon wafers, a task that demands much more power than reticle generation. It is also costly—a system can run as high as \$4 million. Poorly matched to the problem, it forces users to invest too much horsepower for the job. And because of the high defect levels inherent in electron-beam resists, a lengthy inspection and repair loop dominates the electron-beam cycle, making it unsuitable for quick turnaround and rapid throughput. Electron-beam lithography is also incompatible with most existing semiconductor process technologies, requiring manufacturers to replace capital equipment.

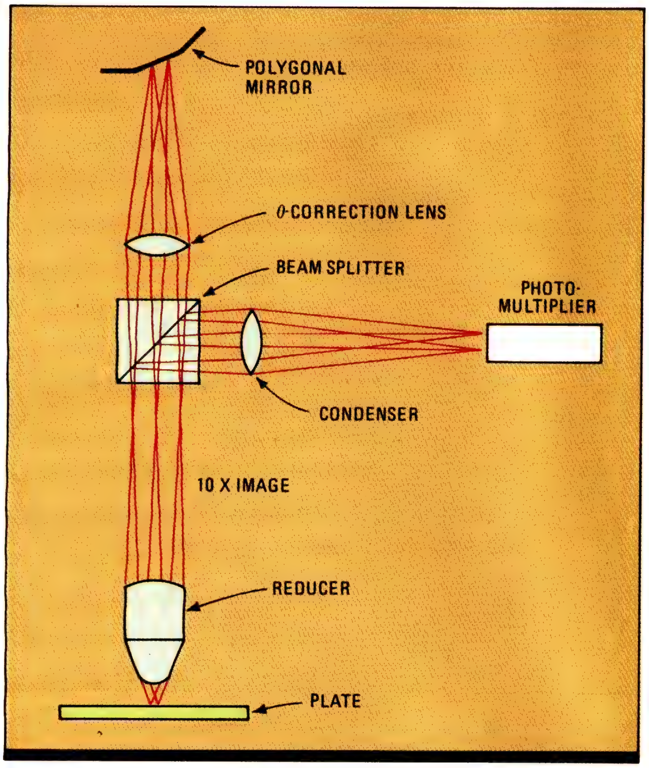
The Ateq reticle writer, on the other hand, uses as its light source a 100-mW argon ion laser, whose wavelength (363.8 nm) and power level match the characteristics of standard optical resists. These are low-defect-density resists, and their use requires only conventional resist-processing equipment.

The Core 2000 has three interlinked control systems—a data-management computer, a rasterizer engine, and a pattern-delivery system controller. The data-management machine, a Masscomp superminicomputer, and the rasterizer engine manage the data flow and generate the video signals used for modulating the laser. The pattern-delivery system controls the printing mechanism in real time.

The data-management computer receives computerized circuit layouts of IC designs in the Electron Beam Engraving System format. EBES is a data format optimized for digital raster generation created by AT&T Bell Laboratories. It is now the standard for virtually all raster-scan electron-beam lithography systems currently available. The data-management computer reads the EBES geometry data and automatically sorts the information according to a strategy for optimal printing speed. The sorted data is



2. LASER-SCANNED. In the new reticle writer, an argon ion laser's beam is used as the energy source. The beam is split into eight paths and fed into an acousto-optical modulator. A polygonal mirror scans the brush of beams through additional optics to the reticle's surface.



3. BUILT-IN CALIBRATION. A calibration system is built into the reticle writer's optics, consisting of a beam splitter at the intermediate image to direct a portion of the scanned beam to photocells that sense the beam position for control purposes.

then stored on a high-speed disk drive.

The rasterizer engine, a powerful digital state machine, receives the data during printing. It also generates the video signals that modulate the Core 2000's eight laser beams, concurrently with the scanning process. The rasterizer engine, based on custom VLSI chips, can achieve rasterization rates of up to 2 million geometries per second. It produces video at the printing rate of 400 megapixels per second. By comparison, typical electron-beam data rates are 80 megapixels per second.

A network of dedicated microcomputers control the pattern-delivery system in real time. The pattern-delivery system also contains a motion-control subsystem to maintain accurate positioning of the eight laser beams on the reticle. This is done through tight interactions among the laser interferometer, beam-position photodetectors, the polygonal-mirror rotation control, X-Y stage position and velocity control, and a fine-correction beam-steering mirror.

Equally as important as the high-speed computational electronic circuitry of the reticle writer is the precise combination of laser, optical, and mechanical techniques in the optical train. The entire optical train of the Ateq system is housed in a rigid cast-aluminum structure called the bridge, which is itself mounted on a block of granite so that differential expansions do not distort the structure.

THE OPTICAL BRUSH

An optical splitter breaks up the laser beam into the brush of eight parallel beams. The resulting multiple beams then go to an acousto-optical modulator, where separate transducers modulate each of the beams independently. The modulator, in turn, is controlled by eight parallel video signals from the rasterizer engine.

Following modulation, fine correction of the laser image position is done with a piezoelectric steering mirror controlled in real time by the motion-control system. A zoom optics assembly takes the position-corrected laser beams and enlarges or reduces the brush image to get larger or smaller printing pitches.

Laser scanning is accomplished by reflecting the multiple beams from a rotating polygonal mirror. The beam path undergoes an angular displacement proportional to the rotation angle (theta) of the mirror. To achieve 0.01-μm accuracy at the reticle image, the dimensional accuracy of the polygon must be held to about one part in 100,000. A theta-correction lens transforms the brush's angular displacement to a position displacement, producing a 10×, flat-field, intermediate image plane.

At this point, a splitter directs a portion of the scanned beam to photosensors to sense the beam's position relative to the slow axis of the stage (Fig. 3). These signals are used to make fine corrections to the modulation timing. The other side of the splitter is used to tap the reflected image from the reticle for calibration sensors. Finally, a reduction lens reduces the 10× intermediate image to a 1× pattern for reticle generation.

Overall performance of the optical system gives imaging accuracy of better than 0.05 μm over the entire 2-mm field at the reticle. This compares favorably with the write-scan linearity of electron-beam systems.

Two IBM Corp. Personal Computer/XTs used as work stations provide user-friendly control of the system. The job-control work station supports the design of reticles. A menu-driven command and data-entry sytem provides an easy-to-use mechanism for rapid generation and modification of the system job control. On-screen graphic representation of the reticle image ensures correct placement of patterns, references, labels, and other objects. This station is independent of the reticle writer and thus can be used off-line. The system executive, built into the electronics cabinet, is the integrated console for the machine and supports all machine operations through a menu-driven command system.

Printing jobs typically begin with the receipt of EBES pattern files representing all reticles required for processing an IC design. The job control is created on the PC/XT any time prior to printing the plate, and the pattern files are copied from tape to the reticle-writer disk. When the plates are to be written, the job-control file is transferred to the reticle writer. Printing an entire set of reticles is done automatically—the operator intervenes only if some action is required, such as reloading reticle cassettes or mounting pattern-file tapes if they have not been previously transferred to the system disk. Nominal turnaround time is less than 30 min per reticle.

The Core 2000 prints patterns up to 5 in.^{2} on a 6-in. reticle at a nominal grid pitch of 0.5 μm and achieves a nominal feature size of 2 μm. The printing pitch is continuously variable so that the image can be scaled from 80% to 105% of nominal. Overlay and placement accuracy are both ±0.25 μm. An automatic coordinate-measurement system facilitates rapid installation, calibration, and service, thus making the reticle writer one of the easiest lithography tools to set up and operate.

An integral laminar-flow air conditioner ensures a particle-free temperature-stabilized operating environment. The optomechanical assembly (print-head) takes up about 34 ft^2, about the footprint of an optical stepper. The electronics-computer cabinet and console area occupies 24 ft^2.

Ateq will start taking orders for the reticle writer this month and expects that initial production shipments will begin in early 1986. The system's price will be about $1.6 million. This compares with the $3 million to $4 million for a comparable electron-beam mask-making system, which also entails a very large setup cost and the added expense of a special room solely for the electron-beam system. ☐

THE TRANSPUTER SPAWNS A RADICALLY NEW COMPUTER

A MATRIX OF THE NEW MICROPROCESSORS RUNS ENGINE AT 750 MIPS

The transputer, the new type of microprocessor developed by Inmos International plc, has found fertile soil in which to sprout: the Computing Surface, a powerful and highly modular computing engine developed by Meiko Ltd. The new offering exploits the transputer's architectural features to build low-cost systems that perform at supercomputer speeds. These systems represent a radical departure from the conventional bus-oriented computer: instead of sharing a bus, individual transputers communicate through private point-to-point links. Meiko uses all four links to each transputer to build a powerful interconnected matrix of several hundred processors.

The major advantage of this arrangement is that every extra processor adds 5 megabytes/s of communications bandwidth, and theoretically there is no limit to the number of processors that can be added in a system. By contrast, a bus-structured multiprocessor has a fixed communications bandwidth set by the data-transfer rate of the common bus, and this limits the number of processors that can be tied together.

The system fits into a compact Hewlett-Packard Co. disk-drive cabinet and typically processes about 750 million instructions per second. This performance puts the Computing Surface into the league of supercomputer systems that cost many millions, yet it will sell for between $220,000 and $300,000, depending on the configuration. A demonstration system, introduced by the Bristol, England, company in July at Siggraph '85 in San Francisco, was built from prototype 16-bit Inmos T212 transputer chips, but the fully engineered version would be based on the T414 32-bit processor, which is just becoming available.

The Computing Surface can be configured for a variety of applications by plugging the appropriate combination of processor, storage, input/output, and other boards into a 40-slot extended Eurocard cage. Other boards, including a floating-point processor, will be added later. A 750-mips system would contain 40 boards with 128 transputers.

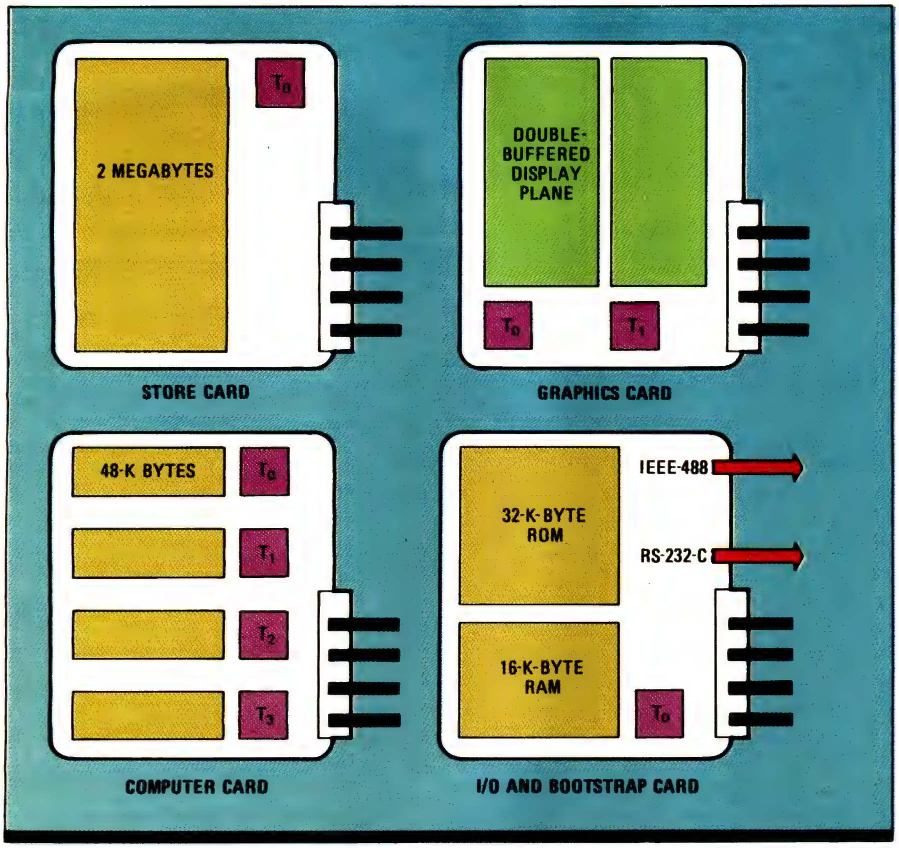
The typical user of a Computing Surface, says Meiko cofounder Miles Chesney, is a Digital Equipment Corp. VAX user who needs the power of a Cray Research Inc. supercomputer [*Electronics*, June 17, 1985, p. 31]. The Computing Surface could tackle computation-intensive problems in physics, meteorology, geophysics, and the like. For these applications, it would likely run as an attached processor to a host machine. Any of a multitude of hosts could drive the machine, including systems based on Q-bus, Unibus, VMEbus, and Multibus, as well as an Apple Computer Inc. Macintosh or an IBM Corp. Personal Computer. Meiko provides bootstrap firmware for this purpose.

Other potential customers are equipment manufacturers that need to build large amounts of processing power into their systems at low cost. In the electronics industry, the Computing Surface could be used in high-performance computer-aided-design work stations, in circuit simulators, and in hardware accelerators. For mechanical designers, the system can produce lifelike solid models of new products. Outside the industry, it has the power to generate animated video displays for cinema and TV or in flight-training and industrial simulators. And the Computing Surface has the processing power needed for future artificial-intelligence applications.

Meiko is uniquely qualified to develop hardware based on the transputer. Its six founders all came from Inmos, where they were heavily involved in the transputer project. Meiko continues to work closely with Inmos; the two even share the same building. "We believe in the transputer. We know it works, so we do not have a credibility problem to overcome," says Chesney. "We spent five years thinking about how to use transputers." The result: Meiko designed the Computing Surface from scratch in just nine weeks. "We did it fast because we knew how to do it."

The idea behind the transputer is to provide systems design-

FLIGHT OF FANCY. As a demonstration, the Computer Surface was programmed to produce a three-dimensional animated trip over and through the surface of a transputer chip. The simulation program was derived from mask tapes used to produce the transputer chips.



1. SURFACE COMPONENTS. Four standard cards, each based on transputer processors, form the modules with which the Computer Surface is implemented. A Eurocard cage holds up to 40 such cards, which can be interconnected through a motherboard to suit specific applications.

ers with a building-block component that can be used in large numbers to construct extremely high-performance systems [*Electronics*, Nov. 17, 1983, p. 109]. Its strength is that it allows parallel connection without the overhead that results from having to provide the complex communication between conventional parallel processors. The transputer consists of a reduced-instruction-set-computer processor with a 6-mips instruction rate, together with hardware features to support parallel processing. The processor incorporates either 2- or 4-K bytes of on-chip memory, which can be extended off-chip through a special interface. Data transfers between processor and off-chip random-access memory may be made at up to 26 megabytes per second. Providing each processor with its own private memory eliminates the processor-to-memory bottleneck of a conventional centralized setup.

HIGH-SPEED LINKS

The transputer incorporates four high-speed serial-communications links that transfer messages between transputers. These links operate concurrently with the processors, providing a combined data-transfer rate in excess of 5 megabytes per second. At the software level, the transputer is designed to efficiently compile high-level languages, particularly Occam [*Electronics*, Nov. 30, 1982, p. 89]. The language describes both software and hardware systems in terms of their constituent processes and formalizes the transfer of messages between them. Messages are dispatched between processes—basically self-contained chunks of program code—by naming the channel that links them.

If the processes are on the same chip, this involves a block move in memory; if they are on different chips, data passes through a channel. In either case, the same machine instruction is used. Processes are held automatically while the transfer takes place, and are rescheduled automatically when it completes the task. There are no interrupts in the conventional sense, and so no time is wasted handling them.

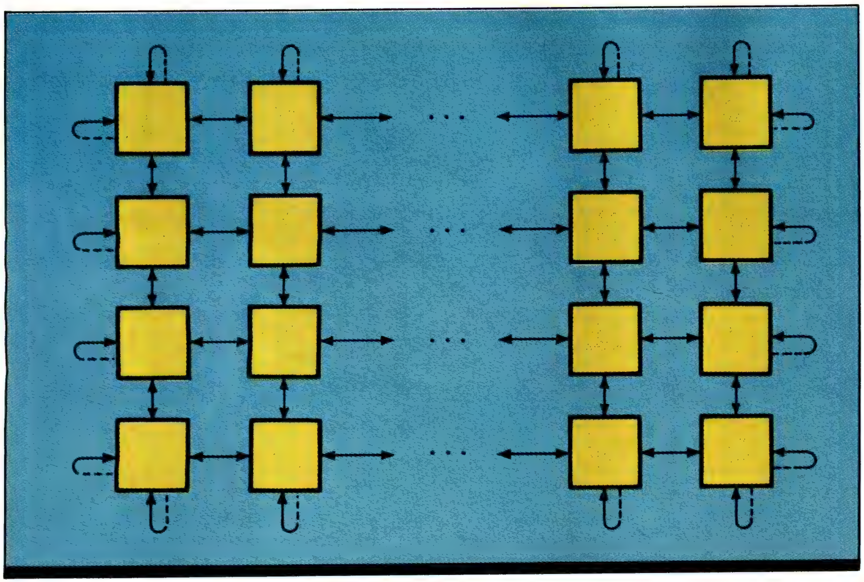
Because of the design of Occam and the transputer, a group of processes will run exactly the same—except for speed—no matter how they are distributed among processors. This means that a system can first be specified in Occam and then mapped directly into silicon, using any number of transputers. In a minimal system, all processes can be executed on a single transputer. But for improved performance, several transputers can be used with one process per transputer. The serial-communications links between transputers are the hardware embodiment of the channel.

Meiko translates this architectural concept into the Computing Surface, which is built up from a basic set of four standard cards (Fig. 1). The computer card carries four transputers, together with 48-K bytes of static RAM. The storage card holds 2 megabytes of 120-ns dynamic RAM and one transputer controller. The graphics card carries two transputers, each with 16-K bytes of SRAM, four NEC Corp. 7220 graphics controllers, and the new Inmos G170 color look-up chip, which can directly drive a raster video system. The I/O card holds one processor, 16-K bytes of SRAM, and 32-K bytes of erasable programmable read-only memory. There are also two RS-232-C ports and an IEEE-488 interface. Other cards—such as a floating-point processor—built around the Weitek Corp. floating-point chip set will be added progressively to the system. A double Eurocard cage holds up to 40 system cards. A common interconnection format ensures board interchangeability. The motherboard carries a power supply and a supervisory bus to all cards in the system.

The I/O card bootstraps the processor into life and supervises its operations. When bootstrapping, it loads code from the program-development environment and routes it through the network of transputer links to the appropriate processors. It also controls the supervisor bus, checking what type of board is in each slot. Finally, it collects hardware-error reports—for example, a parity failure occurring in one of the system's many private memories. It locates faults by board, processor, and even address. After it flags an error, the I/O board also resets individual boards or the entire system.

'TELEPHONE EXCHANGE'

The motherboard is also used to configure the transputer array to suit a specific data-processing application. Transputer links on individual processor boards are terminated in an emitter-coupled-logic driver and brought out to the backplane. The transputer array can then be configured manually using twisted-pair links. Later versions of the machine will be electrically configurable. Custom chips on the motherboard will set up semipermanent point-to-point links between neighboring processor boards. "The motherboard will act as a telephone exchange," says Chesney. "At the moment, we are in the era of manual plugging, and that is the most flexible. Within the short development cycle, there just was not time to develop an electrically configurable version. The board will be divided into domains, or self-contained processor blocks, with

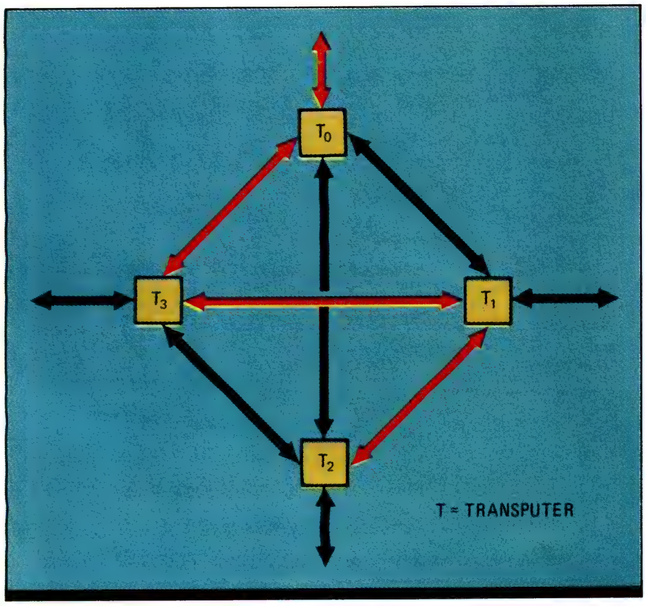


2. INTERCONNECTION. Connections through a backplane or motherboard create a 4-by-10 matrix of cards; the cards each contain four transputers. Any or all of the links can connect to any other point to the backplane, and the network can be connected to other matrices.

gateways between the domains."

The hardware setup provides users with a complex interconnected processor network. On each processor card, all four transputers are linked together by three of their four communications channels. The four remaining links are used to interconnect boards, creating in effect a board-level supertransputer. "We have implemented one level of hardware nesting," says Chesney. The backplane connects processor boards to form a 10-by-4-board rectangular array (Fig. 2). Any or all of the links may be reconfigured to connect any other point on the backplane. The network can be extended with connecting links between cabinets.

Nevertheless, connecting many transputers together does not guarantee performance; the setup must be matched to the data-processing task in such a way that every processor is used efficiently. An example is the display demonstration shown last week at Inmos' press conference announcing the availability of the IMS T414 transputer. Though it was not intended as a serious application, it was designed to show the power of the machine in performing a nontrivial task. In this case, the demonstration unit was programmed to generate an animated three-dimensional color representation of the transputer surface (see photograph, p. 43).



3. PIPELINE CONNECTIONS. On the Meiko processor card, four transputers can be linked up by their serial-communication channels. A pipeline is formed by passing data in a zigzag from transputer to transputer through addressable channels, as shown by the color path.

The data base of the IMS T414 is loaded into Meiko's Computing Surface as a hierarchical set of definitions of cell layouts, exactly as used to generate the device's electron-beam mask tapes. This occupies about 20 megabytes of DRAM, so 12 storage cards, each with 2 megabytes of memory, are first plugged into the processor.

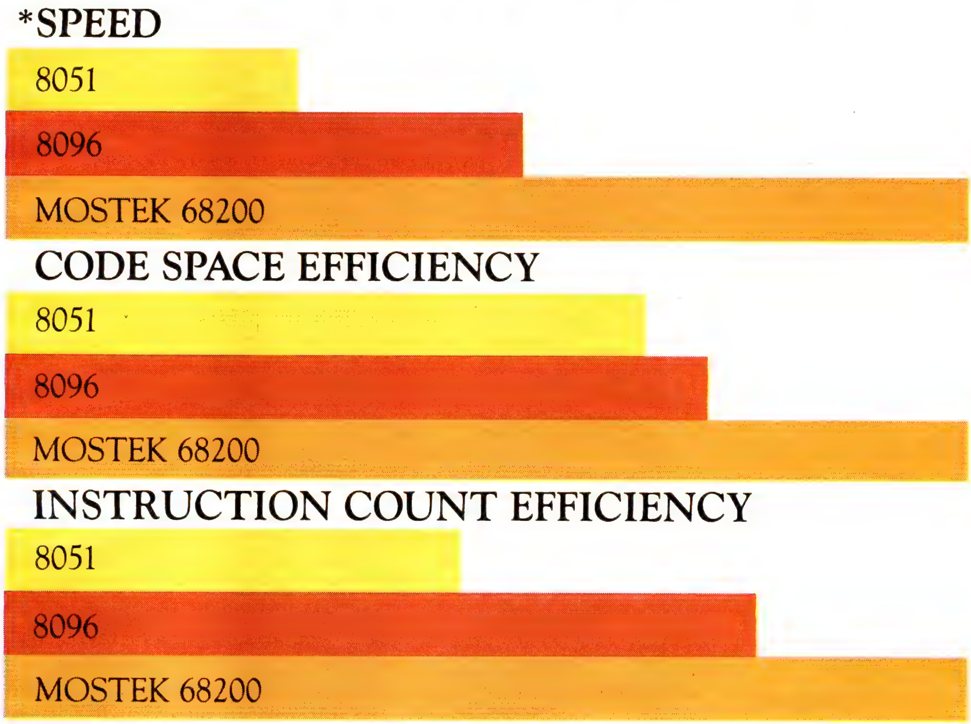
To turn this data into an animated image requires a tremendous amount of processing power, so the task is split between five processor pipelines working in parallel. Pipelines, or data-processing production lines with transputers working in series, are formed at the board level by using the transputer's communications links in a zigzag sequence (Fig. 3) and by connecting the links between boards. When the program is running, the user can view the entire chip surface or zoom into the smallest transistor building-block structure, called a leaf cell. The magnification scale sets the amount of chip surface that can be viewed through the screen window, and the task of working this out is allocated to one of the pipelines. Data describing the remainder of the chip is then discarded.

First, the selected data generates a two-dimensional model of the transputer's four metal and polysilicon interconnection layers. The four remaining processor pipelines working in parallel turn the hierarchical circuit description into a 3-d perspective view; each pipeline handles a quarter of the image. Stages of the pipeline that involve complex and lengthy computations are further replicated to increase concurrency. In particular, depth sorting—deciding which mask areas are concealed by intervening layers—is particularly processor-intensive. So by replicating this stage, its throughput can be matched to other stages in the pipeline. The last pipeline operation is to fragment the image into elemental building-block shapes, or trapezoids. The graphics board accepts these and assembles them into the complete image (computer-generated mask data is fragmented in much the same way).

The Inmos Transputer Development System is used to program the machine. It is currently hosted by a VAX running under the VMS operating system, an IBM Personal Computer AT, or a 68000-based development host marketed by Inmos. The TDS supports the Occam programming language, and Inmos is planning to make Fortran, C, and Pascal compilers available at the end of the year. Chesney believes that it will be possible to transfer existing applications—written in conventional languages—to the Computing Surface. Individual program segments, written in Fortran, could be allocated to specific processors. Occam would then be used to handle the transfer of data between program segments.

For new applications, programmers would be able to exploit concurrency by writing their applications in their own notations for concurrency, and then implementing them in Occam. Chesney admits that programming is now the major hurdle in the way of putting the Computing Surface to work. "The use of a concurrent programming model is a new style of working for programmers. It means learning new skills, but those that rise to the challenge can reap the benefits of access to enormous computing power." □

ANYTHING E



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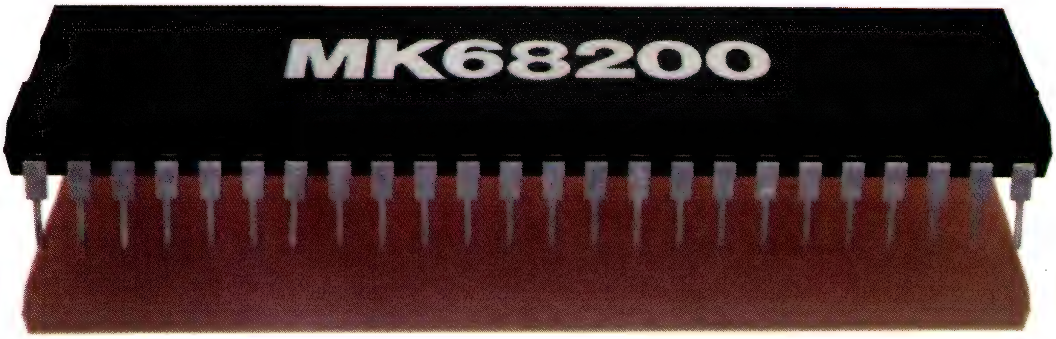

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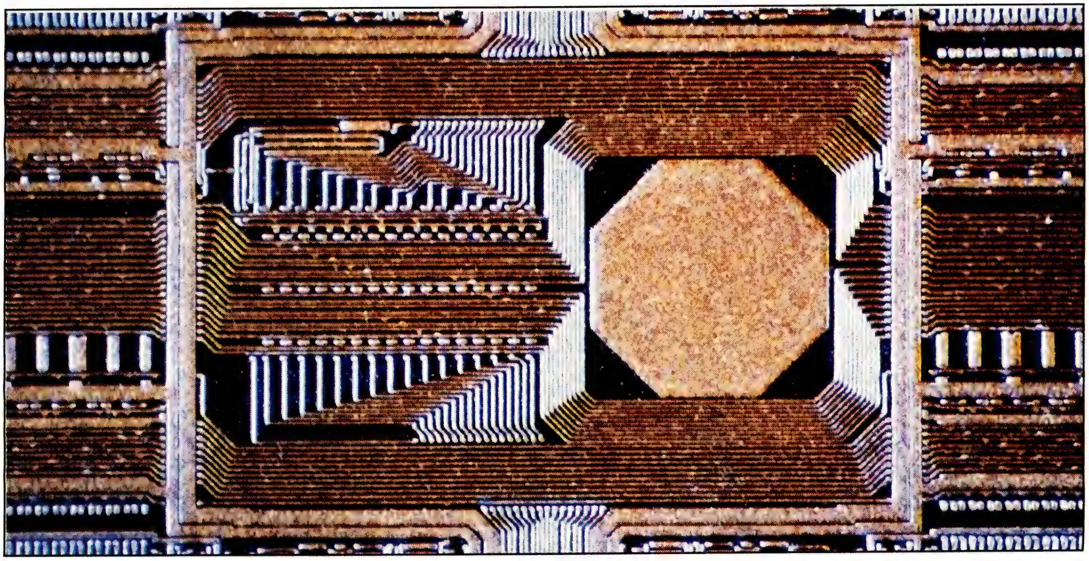
TECHNOLOGY UPDATE

1

COMPUTERS

THE PACE IS ACCELERATING

by Tom Manuel



This article launches *Electronics*' 11th annual Technology Update, a comprehensive analysis by the editors of major worldwide trends in key segments of electronic technology. In computers, scalable architecture, multiprocessing, and reduced-instruction-set designs lead the list. Upcoming articles in the five-part series will cover semiconductors, communications, manufacturing, and consumer electronics.

The pace of technology has accelerated in computers. Hectic worldwide competition has fueled a rich technical creativity: major developments are a daily occurrence and will continue at the same or an accelerated clip. The U. S. has led the technological race from the start, but Western Europe has never lagged far behind, and Japan in recent years has begun to catch up. Now several other Asian countries are about to jump into the fray. Though IBM Corp. dominates world markets, competition to develop new technology remains fierce because the huge market carries even bigger potential. Despite the present slowdown, the industry is on its way to becoming the second biggest business in the world after agriculture.

Several major trends in computer technology are developing. One is the big drive to scalable unified architectures—designs that can be expanded in stages from small systems to very large-scale computers without requiring changes to memory subsystems, peripherals, or software. Most computer systems in the next two to five years will be of this type. There will be two levels of scalability: a hierarchy of interconnected systems and extendable machine families at each level of the hierarchy.

Supporting this trend to scalable computer systems is the rapidly accelerating development of parallel processing. With many companies now moving into parallel processing, it is clear that parallel processing—or multiprocessing—is the wave of the future. With the advent of microprocessors with mainframe power and memory chips with the capacity of entire memory systems, modularity and scalability in both processing logic and storage are easier and much less costly to build.

Another highly visible trend in computers today is the reduced-instruction-set-computer architecture. Among the fundamental RISC concepts, three stand out: machine instructions should be simple; most instructions should be constrained to execute in one clock cycle; and a large set of fast registers should be provided to allow as many instructions as possible to execute among registers without going to main memory. The primary goal in RISC designs is to build faster single processors. RISC processors, of course, can be used in parallel-processing computers.

A small but increasingly important trend is the development of language-specific integrated-circuit processors. Processors are available or under development for several high-level languages, including Ada, Forth, Lisp, PL-1, and Prolog. Another force to be reckoned with is the artificial-intelligence gold rush. Every company seems to be jumping on the AI bandwagon. In the realm of data storage, the hot new technology is optical storage. But its older brother, magnetic storage, is far from extinct or even out of date.

ALL TOGETHER NOW

In two years, multiprocessor parallel machines will be everywhere. Nearly all machines except the low-end work stations will have some form of parallelism. There are two yardsticks with which to measure parallel machines: graininess and levels. Grain defines the size of the entities being duplicated; a parallel computer has either fine- or coarse-grained parallel architecture. The other method is to define at what level, or levels, of a system's hierarchy parallelism is injected.

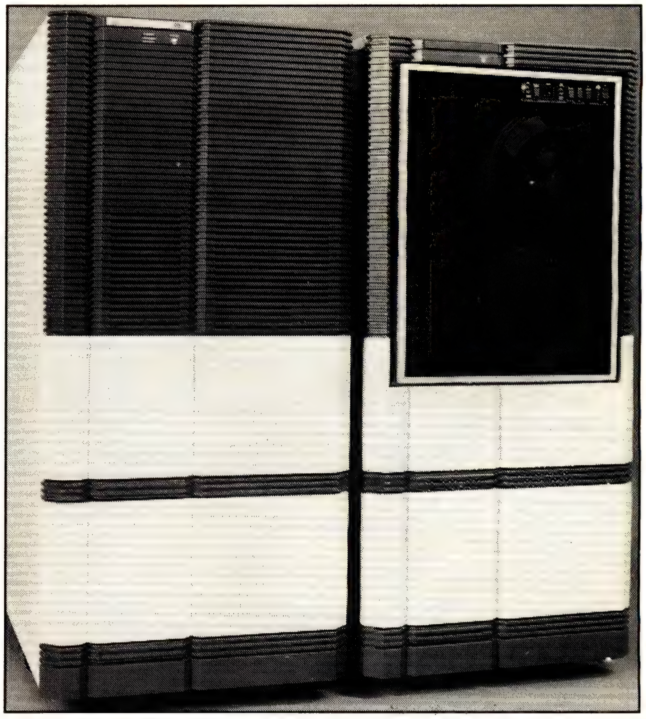
Grain size is the period between synchronization events for multiprocessors or processing elements, according to C. Gordon Bell, vice chairman of technology at Encore Computer Corp. in Marlboro, Mass. Bell has developed a four-level grain classification of the degrees of parallelism. Mentor Graphics Corp., among others, has classified parallel-processing computers as either having high-level or low-level parallelism.

Fine-grain parallelism is that which is inherent in a single instruction or data stream with synchronization being done at a level of one instruction, as in pipeline machine designs and systolic array processors. Medium grain is parallel processing or multitasking within a single process, a synchronization level of 20 to 200 instructions. Coarse-grain parallel processing is the multiprocessing of concurrent processes in a multiprogramming environment—200 to 2,000 instructions.

Nearly all machines will have some form of parallelism

Encore's Multimax parallel computer does both medium- and coarse-grain parallel processing as Bell defines them. Distributed processing across networked computers to form a single computing environment is very coarse-grain parallelism, Bell says. The synchronization level is from 2,000 to 1 million instructions. Representative systems exhibiting very coarse-grain parallelism are clusters of Apollo Computer's Domain work stations, Digital Equipment's VAX 8600s, and Sun Microsystems' Ethernet-based Sun Workstations. Multiple Encore Multimaxes on Ethernet and many other distributed-processing systems also demonstrate very coarse-grain parallelism because the work nodes in such networks can form single computing environments.

"In high-level parallelism, multiple processes are executed at once. Parallelism must be explicit at source-code level, usually requiring language extensions, and the processes must be synchronized externally in most systems by rewriting the code," says Michael R. Butts, engineering manager at Mentor's Computer Systems Division. But in low-level parallelism, primitive operations—basic processing functions—are executed at once, Butts says. Parallelism is detected by an optimizing compiler in existing source code written in standard languages, he explains. Since the parallelism is below the process level, no synchronization is required, he says.



DOUBLE RISC. The Pyramid 98x Isoprocessor superminicomputer uses two identical reduced-instruction-set processors.

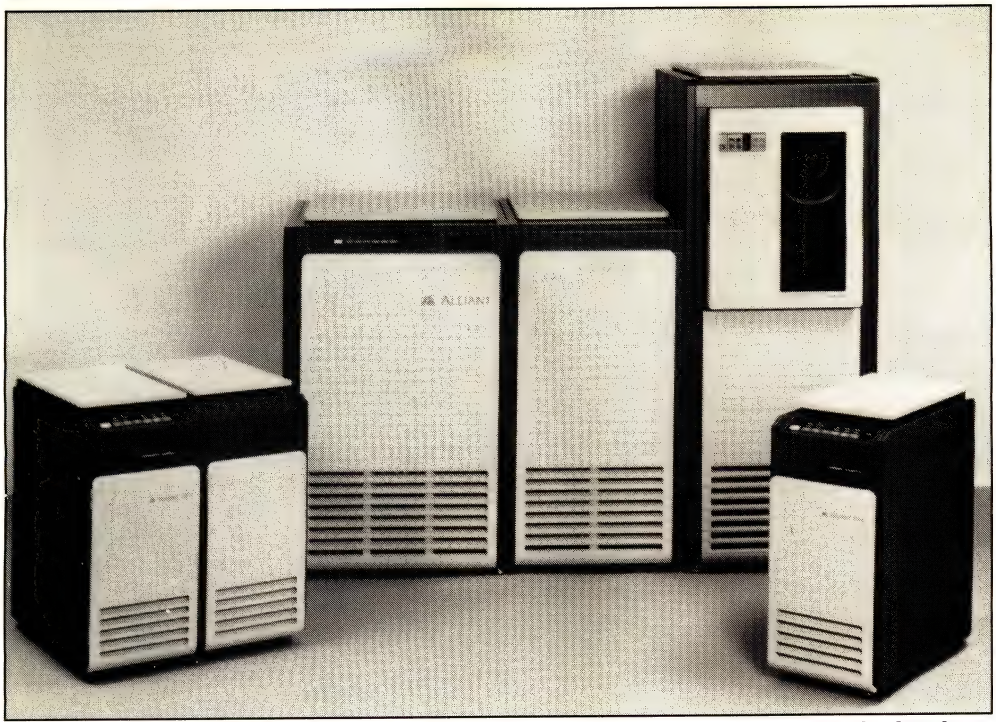
Many companies have been jumping on the parallel-processing bandwagon recently with products in the middle-grain category. Companies such as Cray Research, Denelcor, Elxsi, and Perkin-Elmer have sold parallel multiprocessors for several years. Other companies announcing parallel computers include Sequent Computer Systems; Flexible Computer; Masscomp; Intel; Pyramid Technology; Bolt, Beranek & Newman; Meiko (see related story, p. 43); Alliant Computer; ICON Systems and Software; and IBM.

Further, universities worldwide are researching many advanced parallel-processing designs. Also working on parallel processing are big national projects such as the Institute for New Generation Computer Technology (ICOT) in Japan, the Alvey project in Great Britain, Esprit in the European Communities, and the privately funded Microelectronics & Computer Technology Corp. Consortium in the U. S. ICOT has three different prototytpe parallel machines in one lab, providing an excellent means to compare and contrast approaches to the technology.

But few commercial systems today are in the fine-grain multiprocessor area compared with the number of low-level parallel architectures in supercomputers, mainframes, and slightly more specialized machines such as Mentor's Compute Engine accelerator [*Electronics*, Sept. 30, 1985, p. 30].

Other designs in this fine-grain area are described as massively parallel. For example, Thinking Machines Corp., Cambridge, Mass. is aiming its Connection Machine to fill that gap. A prototype of the machine using 64,000 one-bit processors and executing 1 billion operations/s will be ready to deliver to the Defense Advanced Research Projects Agency by year end. The 64,000-processor prototype is a steppingstone to a million-element model. Other massively parallel machine projects are under way [*ElectronicsWeek*, April 22, 1985, p. 36] and several machines will surface within a year or two. Such designs will be commonplace by the mid 1990s.

Computer designers have found it quite easy to build a variety of parallel hardware architectures. But to make parallel processing work, software technology must catch up. The



TWO WAYS. Alliant's FX/8 field-expandable supercomputer applies parallel processing two ways: it can have up to an eight-processor complex for computation-intensive jobs and up to 12 processors for interactive ones.

process, already under way, will accelerate in the next few years. More compilers will be developed that automatically make application programs parallel. Alliant Computer Corp.'s Fortran compiler, for example, automatically sets up Do loops for parallel execution. Mentor's C compiler for the Compute Engine generates machine instructions that make maximum use of the elements in the processor's low-level parallel structure.

In the supercomputer realm, machines from Cray Research Inc., ETA Systems, and Convex Computer Corp. in the U. S. and from the three major Japanese computer companies—Fujitsu, Hitachi, and NEC—sport optimizing compilers that take the machines' low-level parallel architectures into account. Now the smaller parallel computers will be getting at least this level of compiler technology, and some will get advanced parallel compilers. Pushing the state of the art of supercomputer compiler technology hard are the many startup minisupercomputer companies, such as Convex, Floating Point Systems, and Scientific Computer Systems, along with Alliant, Mentor, and Sequent.

The key to RISC is in the compiler technology

Development of parallel-computer architecture is being pushed from both ends—bottom up and top down, says Dave Rodgers, Sequent Computer Systems Inc.'s vice president of engineering. "Microcomputers have become powerful and cheap enough to easily stack them up in parallel systems to reap great price/performance benefits and a broad range of scalability," Rodgers says. "The top-down push, though less visible, offers a spurt in the development on parallel architectures and algorithms resulting from the decrease in the rate of improvements in the speed of single processors at the very high end."

Because supercomputer research and development often gets military and other government funding, much of the work is done at public expense. "The results become available for the low-end systems, and a whole new set of applications becomes feasible without great development expense," Rodgers says.

RISC architectures also require software developments to realize their full potential. Compilers must be rewritten to produce efficient code for these machines. For example, compilers have to be smart enough to take advantage of register-to-register operations and the simple one-cycle instructions.

RISC designs came into being after computer scientists analyzed billions of machine instructions from billions of lines of high-level language code and discovered that simple instructions, such as Branch, Load, Store, and Add, were used constantly. Complex instructions, however, rarely saw use.

Astute computer researchers recognized an opportunity here (see "Developers stay happy in academia as RISC goes commercial," p. 53). Since the simple instructions, except those that load and store from memory, could be executed directly in one machine cycle, there is no justification to execute them interpretatively in microcode, which usually takes several machine cycles. From this simple discovery RISC was born. Besides this primitive-instruction idea, many additional ideas have been added to the RISC concept.

Recent developments in circuit technology and economics provide a kicker for RISC, according to Sequent's Rodgers. "Certain structures on silicon are expensive, while others are not. The cost tradeoffs in hardware are different now than they used to be," he says. For example, very high-speed memory chips, which can be used to build many high-speed registers, are cheaper now than microcode. So it makes sense to invest system costs in large register sets instead of microcode.

To develop a whole new product line using RISC concepts, Hewlett-Packard Co. hired as its chief researcher the first manager of the first RISC project—the 801 project at IBM—Joel S. Birnbaum. In a paper entitled "Beyond RISC: High-Precision Architecture," HP Laboratories chief Birnbaum and co-author William S. Worley Jr., also of HP, put it this way: "A computer whose fastest level of the storage hierarchy is general-purpose registers has several advantages. The obvious one is that register-to-register instructions are intrinsically faster than those requiring main storage access. Another is that modern compilers can analyze data and control flows and can thus allocate registers efficiently."

But can all the compilers that are needed in a complex system built with simple RISC-based processors now do this effectively? "The key to RISC is all in the compiler technology. The people who will be most successful with RISC will have multilanguage front ends to a common RISC-oriented back-end compiler," says Rodgers of Sequent.

System designers, of course, can use RISC processors in parallel architectures to produce ever-faster computers at lower cost. Other companies dabbling in RISC or RISC-like machines are Acorn Computers, Harris, IBM, MIPS Computer Systems, Ridge Computers, and Saturn Computers.

Gurus of high-level-language compilers are taking a good look at other avenues besides RISC and parallelism to speed up the processing of programs written in their favorite languages. They plan to take advantage of the speedy development of very large-scale-integration application-specific ICs by developing language-specific chips.

One example of this trend is the IC Forth engine developed by Novix Inc. and available as a prototype from the Cupertino, Calif., company. Its parallel architecture and minimal hardware is implemented with 8-MHz, 4,000-gate, CMOS arrays. In addition, Texas Instruments Inc., Dallas, is working on a microprogrammed VLSI computer for the Lisp language. Rockwell International Corp., Pittsburgh, has developed a 16-bit CMOS advanced-architecture microprocessor designed to support the execution of such block-structured languages as Ada and PL-1. Many more language-specific computers on a chip will surface in the next few years.

Chip designers are grooming several language chips for AI languages and specialized AI computers. Interest in AI, especially in expert systems, is mushrooming. That interest will continue to grow until every company in the computer industry will be working on AI. One of the most promising aspects of AI is its potential to make computers much easier to work with. Today's so-called user-friendly computers and software are not at all easy to use. For truly widespread use, computers need to become as easy to operate as cars, telephones, TVs, and video cassette recorders.

EASY DOES IT

Big strides have been made in improving ease of use in the last few years. AI programming could mean a quantum leap in friendlier user interfaces. One promising example is the Paradox data-base system from Ansa Software. The Belmont, Calif., company uses AI technology to do program synthesis—turning a user's simple query, in the form of an example, into a complex data-base program—and heuristic query optimization—structuring a query program for maximum performance based on knowledge that the Paradox system has or even has learned from preceding queries.

By using this machine reasoning behind the scenes, the Paradox data-base system hides the real complexity of a powerful relational data-base system for personal computers behind a simple user interface. Users simply display a variety of tables of data through a Lotus 1-2-3-like menu, check off columns, and give examples of the types of information and calculations they want. Paradox software does the rest.

Every company in the computer industry will be working on AI

Paradox is just the tip of the iceberg in what the computer industry must provide in applications that are really easy to use; designers still have a long way to go. AI programming requires a lot of computation and memory resources. The increasing performance and plunging cost of such resources are about to make enough of both available for significant application of AI to user interfaces.

Fast, high-resolution graphics technology is also a powerful tool for better user interfaces. Graphics too is joining the ranks of affordable technology. For example, personal computers built on a processor capable of 1 million to 3 million instructions per second and equipped with 1 megabyte of memory, 80 megabytes of disk storage, graphics, and even an optical compact-disk drive pack enough power for some serious AI-based interfacing. These machines also could do some expert-system programming. Such machines are almost here—some may appear within the next year; machines with twice that performance could arrive in two years.

Expert systems—programs that store and use human knowledge and expertise in a particular field—will be one of the next big markets. One such example is the financial-planning system introduced last month by Applied Expert Systems Inc. of Cambridge, Mass. An example of an expert system that has been in use for some time is the combination XCON and XSEL package used by Digital Equipment Corp. to configure computer systems for customers. In the past few years, many expert-system development tools have been created. In the next few years, these tools will help produce the knowledge bases that are used with inference engines—software that reasons—to become complete expert systems.

PARALLEL. From 2 to 12 NS32032 processors work in parallel in Sequent's Balance 8000. I/O processors balance the machine.

Many domains of knowledge, skills, creative tricks of the trade, and expertise lend themselves to expert systems, which can be used to capture and codify valuable techniques and knowledge. Expert systems, unlike people, can run indefinitely without getting sick or tired. They won't ask for raises or look for better jobs elsewhere. They are also a convenient way to keep expertise and knowledge in a company even when workers leave.

Knowledge bases for expert systems of any consequence will get pretty big—into the tens or hundreds of megabytes or even higher. In addition, other computer users increasingly need access to very large information bases. An emerging technology, optical disk drives, is ready to fill the storage gap created by these new applications. Some of the large information delivery-and-retrieval applications were impractical with magnetic-memory technologies because these applications are best served with very large volumes of information on single small disks that can be easily carried or mailed.

Three types of optical-storage equipment will start to play an important role in information and knowledge-base applications. Compact-disk read-only memory suits information applications, where copies of a high-volume information base need to be distributed to many users, and the base needs occasional updating [*Electronics*, Sept. 16, 1985, p. 26]. Examples are encyclopedias, catalogs, and reference manuals for large systems such as jet aircraft. Information that would require 220,000 printed pages or 1,500 of today's floppy disks can fit on a single CD. Another type of optical-memory technology is a write-once disk that is good for archives. The third technology is based on a combination magneto-optic effect that will produce a read/write optical disk that could start replacing traditional magnetic devices.

CDROMs will be the first optical technology to take off in any sort of mass market, say some industry observers. But the other two types may take off just as quickly, note other market watchers. CDROMs have a strong proponent in Gary

Kildall of Activenture Corp., who is convinced that they will take off in the consumer market within a few months. On the other hand, Jan Lewis of the Palo Alto Research Group believes the technology will go from an innovator's technology to beginning mass-market penetration in a couple of years, but will take a few more years to achieve real mass-market status.

Magnetic-based storage devices, the current mainstay of computer storage, are continuing to advance apace. In the next several years, cost per megabyte will drop just as steadily as capacity per spindle will increase.Both trends will be at the same actual rate as in the past, but actual capacity and price levels are trailing the publicity, says Geoff Seabrook, vice president of planning and product management at Memorex Corp, the Santa Clara, Calif., subsidiary of Burroughs Corp. Though marketing hype claimed 86-megabyte, 5¼-in. drives were available three years ago, delivery was just starting during the second half of this year, he points out.

But a major breakthrough in magnetic recording technology won't come soon, Seabrook says. Developments reaching

DEVELOPERS STAY HAPPY IN ACADEMIA AS RISC GOES COMMERCIAL

by Clifford Barney

The two professors who shook up the computer industry by deciding to speed up central-processor performance using simple, single-cycle instructions are perfectly content to retain their academic vantage point while the concept goes commercial.

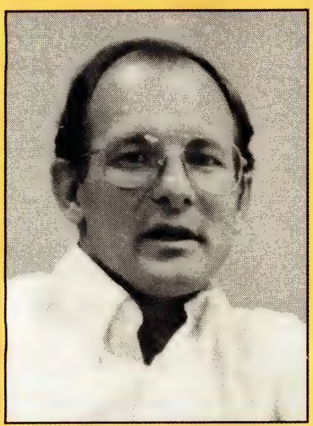
No one is happier than David A. Patterson that the concept of reduced-instruction-set computers has begun to catch on in the computer industry. If it hadn't, says the 37-year-old professor at the University of California at Berkeley, "I might have had to switch careers and start a company. This way I get to stay and do research."

His colleague, Stanford University professor John Hennessey, 32, actually helped start a RISC computer company, MIPS Computer Systems Inc. But this fall, Hennessey returned to Stanford to head its new computer laboratory. Only an irresistible offer to help adapt the multiprocessor without an interlocked pipe stages (MIPS) for a commercial product lured him into business in the first place, he says. Hennessey will be a consultant for the Mountain View, Calif., company while continuing his research on a multiprocessor version of the chip at Stanford.

Hennessey calls himself the "corporate" spokesman for RISC, but says Patterson took the real risks. "Dave did a tremendous service to the community in the beginning by talking about it and standing up to a lot of criticism, some of it vehement," he notes. "A lot of people beat up on him." The reason could be the unorthodox methods Patterson adopted to communicate RISC's advantages.

The Berkeley RISC I chip, for example, carried on its mask set a tiny emblem of a Porsche, Patterson's slightly derisive way of emphasizing RISC's high performance and stripped-down design. His emblem for a complex-instruction-set-computer design was a tail-finned gas guzzler from Detroit.

Patterson also raised some hackles by benchmarking the Berkeley RISC chip against a Digital Equipment Corp. VAX minicomputer and showing up the VAX against the RISC chip. His academic peers, who swore by the VAX, weren't too happy about having their $100,000-plus equipment beaten by a student-designed chip.



DAVID A. PATTERSON

Hennessey, more diplomatic, compared the Stanford MIPS chip to DEC's PDP-10 mainframe, which no one used any longer in 1982, or to Motorola's 68000, which no one had used yet.

But the furor over RISC has died down. "I don't get as many people mad at me any more," says Patterson.

Although Patterson and Hennessey did much to advance the concept, RISC did not originate at Berkeley or Stanford. Its genesis was in building 801 of IBM Corp.'s Thomas J. Watson Research Center in Yorktown Heights, N. Y. The 801 project, an inspiration of IBM researcher John Cocke, began in 1975 with the purpose of developing a computer that executed instructions in a single machine cycle.

IBM's 801 minicomputer never reached the market, but its influence has been considerable. Instructors soon incorporated the basic concepts in graduate courses at Berkeley and Stanford. Patterson's class went on to develop the RISC I, which featured overlapping on-chip registers to save time on procedure calls.

JOHN HENNESSEY

Hennessey's MIPS chip was also chosen to highlight RISC's performance in the range of 2 million to 10 million instructions per second. The software arranges all pipeline interlocks at compile time, allowing the parallel-processing benefits of pipelining without increased hardware complexity.

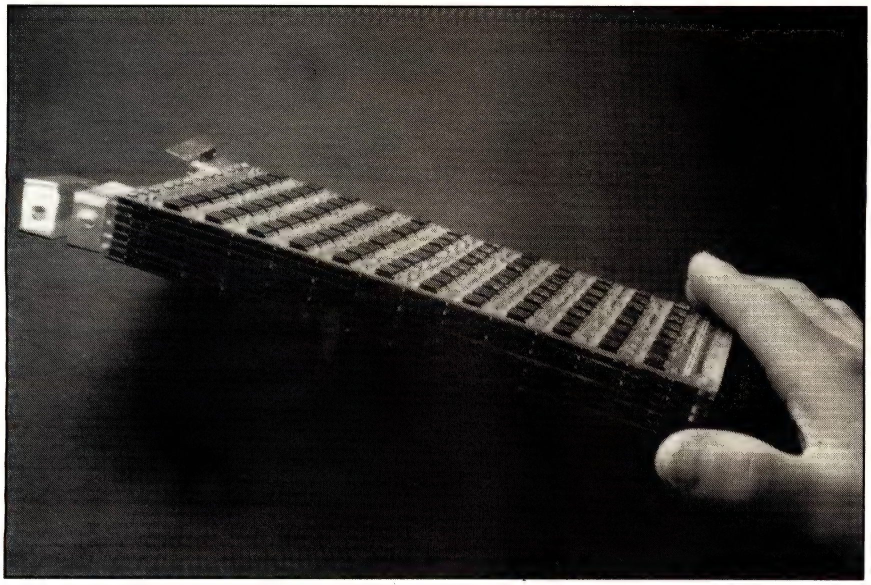
Meanwhile IBM incorporated some of the 801 concepts into its Sierra mainframe. IBM recently announced that its RP3 parallel-processing research machine will be based on a RISC microprocessor. The company is also expected to introduce a work station with a version of the 801 processor this year or early next year.

Other computer and chip manufacturers have slowly lined up behind the idea. Ridge Computers, Santa Clara, Calif., and Pyramid Technology Corp., across the street from MIPS in Mountain View, already market computers that use some RISC concepts. And Hewlett-Packard Co. is transforming its entire product line into equipment based on RISC.

Even DEC, Maynard, Mass., whose VAX is the canonical example of a complex-instruction-set computer, has a RISC project under way. And the Defense Advanced Research Projects Agency is funding research for RISC processors built from gallium arsenide.

All this activity is very satisfying to Patterson and Hennessey, who are now engaged in projects to further develop RISC systems. Hennessey is working on MIPS-X—a wafer-scale packaging technology that will put 10 MIPS chips into a single package. The goal, he says, is to put "a Cray on a desk"—a desktop machine to compete with the Cray supercomputers.

Patterson and his Berkeley colleagues are working on language-specific RISC chips and have already adapted RISC for Smalltalk, an object-oriented language. A Lisp version will be next. ☐



3D. A circuit module eight boards thick in the Cray-2 supercomputer has circuit connections in all three dimensions. Each module has about 750 integrated-circuit packages for a circuit density near 40% ICs by volume.

the market will be "a little bit of everything that has happened in the past—higher track densities and more bits per inch achieved by development of better heads and positioners and advanced media."

SPUTTERED MEDIA

Thin-film metallic media are the development most likely to to push drive density to more bits per inch in the near future. Although the media are not being made in the large production quantities of oxide disks, they are starting to reach the computing mainstream. Domain Technology, for example, is producing and shipping its thin-film metallic disks—nickel-plated with a sputtered carbon overcoat—at the rate of more than 60,000 per month, says David Pearce, president and chief executive officer of the Milpitas, Calif., company. Domain can produce more than 1.2 million disks a year.

A competitor, Lanx Corp., has the capacity to produce half a million completely sputtered 8-in. thin-film disks a year without any plating steps. In addition, the San Jose, Calif., company can make 5¼- and 9-in. disks with its four sputtering machines. Lanx, which started making the first thin-film disks for perpendicular magnetic recording back in 1983, this year introduced sputtered disks for the more common longitudinal recording.

Back in Milpitas, another contender, Komag Inc., which also makes thin-film sputtered disks, has just signed a major contract worth several million dollars with two disk-drive vendors to provide them with media. The company sees the demand for sputtered media accelerating about 12 months ahead of earlier expectations, according to a spokesman.

The sputtering process for manufacturing thin-film disks, compared with electroplating, is a continuous vacuum-deposition process that transfers material atom by atom from the source to the target. It creates a smooth layer whose thickness can be controlled to a fine tolerance. Typically, two layers are sputtered onto the rigid disk substrate. A magnetic layer of metallic nickel as thin as 2 μin. is deposited on the disk surfaces in a process similar to that used to coat semiconductor wafers with thin metallic films. The second layer is a sputtered diamond-hard 1-μin.-thick carbon overcoat to protect the fragile magnetic layer.

Thin-film electroplated metal media have been around longer than sputtered thin-film media. Although the magnetic characteristics of the two media are similar, the sputtering process produces a smoother surface over which the disk drive's read/write heads have to fly. Consequently, the flying heights can be much lower over a sputtered medium than over a plated one. Lower flying heights lead to many more bits per inch stored on the disk. Now that the sputtering process has been perfected and the costs have been reduced, this improved medium should be showing up in a many more disk drives in the next two or three years.

Vertical, or perpendicular, recording technologies, in which the magnetic domains are oriented perpendicularly to the disk surface, were expected to come on strong by now, but they are not really ready for mass production. For hard-disk drives, vertical recording is highly unlikely in the near term, Seabrook says. Vertical-recording floppy disks are probably much closer to reality.

As more and more personal computers carry larger and larger amounts of valuable and often critical data, reliable backup subsystems will become essential. Tape drives are still a big factor in computer peripherals. The major news here is a big move to cartridge drives, especially at the high end, with drives that are compatible with the IBM 3480, which appears to be fast becoming a de facto standard. It is a good match as a dumping and restoring device for the high-end 3380-type disk drives. But reel-to-reel tape drives will carry on for batch processing and traditional tape applications in data processing. Orders may slow a bit but will not dry up suddenly.

At the low end, to back up the coming wave of the 40-, 80-, and 160-megabyte hard-disk drives for personal computers, low-cost tapes drives using 3M Co.'s latest DC2000 40-megabyte ¼-in.-tape cartridge will become one of the peripherals of choice. ☐

SOFTWARE TOOLS ARE MAKING PROGRAMMERS MORE PRODUCTIVE

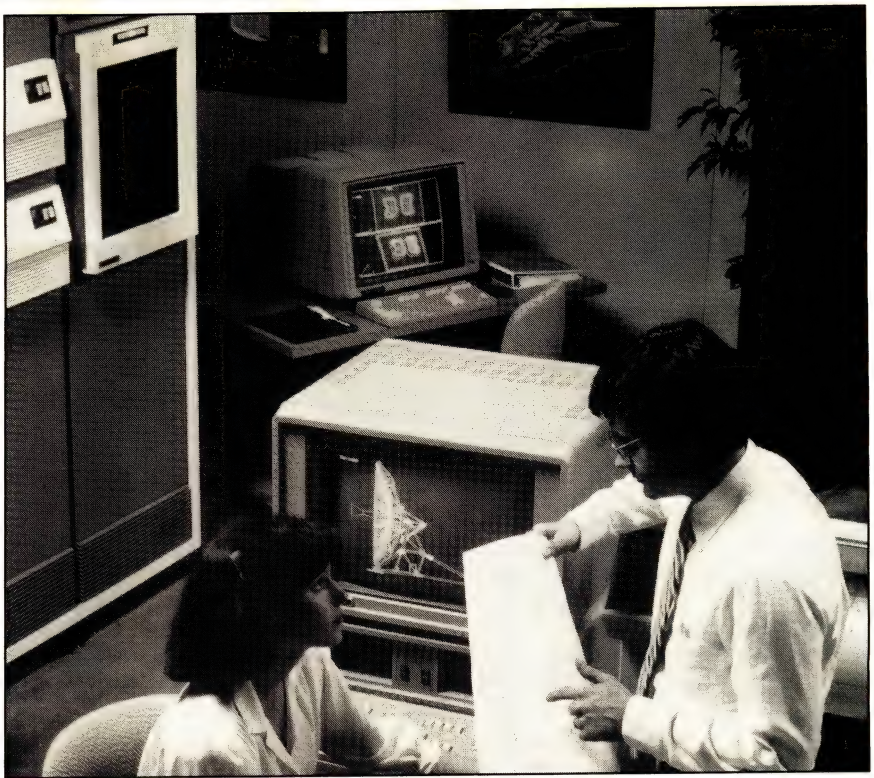
by Alexander Wolfe

Modern software engineering is growing more challenging as electronic systems become more software-intensive. Though the demand for software is increasing 20% to 25% a year, the number of programmers is growing only 5% to 6% annually. The only way to meet the burgeoning need for computer code is to greatly boost programmer productivity.

In the past 12 months, software technology has seen a redoubling of several efforts to beef up programmer performance. More subtly, this ongoing research into formal development methods pushes along software's slow but steady advance from an unstructured art into a refined science.

During the coming year, look for hardware-description languages—software tools to help hardware design. In addition, graphics tools for visual programming and simulation are leading the advanced software technology charge. In the workaday world, acceptance of the Ada programming language is proceeding apace. In living rooms and dens, software-productivity packages—notably word processors and spreadsheets—are heating up the home computer field.

Hardware-description languages are playing a big part in software's upward mobility. Although manufacturers tout



TOOLING UP. Continued refinements in high-level design tools—including description, specification, and *programming languages*—will boost productivity for engineers developing applications software.

these languages as bridging the gap between hardware and software, rather they are programming languages that describe the operation of complex electronic circuits. Hardware-description languages will provide the next generation of advanced computer-aided-engineering tools for integrated-circuit design and will support dense hardware efforts such as the Department of Defense's Very High-Speed Integrated Circuits program.

Work in this area began 10 years ago, spawning a variety of hardware-design languages. Now researchers are trying to develop a standard language.

Indeed, the goal of the VHSIC Hardware Description Language, developed at Intermetrics Inc., "is to define a standard medium of communication among hardware designers," says Roger Lipsett, manager of the language program at the Bethesda, Md., company. A common language would ease issuing of specifications and allow the interchange of designs for second-sourcing. But its biggest benefit is to encourage mastery of the complex very large-scale-IC design process.

"In the past, most hardware-description languages have been fairly low-level, down at the logic-gate level or below," says Lipsett. "That's been suitable in medium-scale integration or large-scale integration. But once you get up to VLSI, where you're talking about designing full computers on a chip and full systems on a board, the level of complexity in a single design is huge. There needs to be some way to describe this information in a way people can understand." Hardware description languages are evolving from gate-level specification tools to more sophisticated programs allowing engineers to design by means of functional descriptions, he notes.

The VHSIC Hardware Description Language is geared for system-level functional and behavioral decriptions while maintaining support of logic-gate-level descriptions. Currently, the language is fully defined. Under DOD contract, Intermetrics is now at work generating software, including a simulator, to support the language. But the language is not geared solely to the Defense Department's VHSIC needs. "There's quite a bit of interest in it in industry as well," says Lipsett. "The language definition itself is, for all practical purposes, in the public domain."

SEEING THINGS

Some important software tools enable engineers to clearly visualize the operation of their programs. Two of these graphics techniques are coming to the fore. Visual programming is the subject of several serious research efforts. Visual simulation has arrived in the Performance Analysis Workstation, developed at AT&T Bell Laboratories, Holmdel, N.J. The work station is available as part of AT&T's Unix Toolchest.

"The idea is to make the thinking process of the engineer as close as possible to the implementation process," says Benjamin Melamed, a member of AT&T Bell Labs' Performance Analysis Studies Group that developed the work station. "Instead of having to write a piece of code, which involves considerable abstracting of the conceptual model, visual programming and simulation allows the engineer to sit down and draw the system the way he would naturally think of it."

Visual simulation is used to model computer, communications, and manufacturing systems. Programmers can monitor the flow of a program on screen and watch operations move from node to node. Statistics such as histograms and time series also appear on screen. The technique promises aid in design analysis, debugging, and program verification.

But visual tools will not necessarily replace high-level languages, says Robert Morris, supervisor of the Performance Analysis Studies Group. "I think that they're one of an armory of tools which the future programmer will want to have at his disposal." Morris won't reveal new Bell Lab's visual-simulation research efforts but adds, "we're trying to make our tools more general and more flexible than they have been in the past."

Recent visual programming innovations are the Computer Corp. of America's Program Visualization environment; the University of California at Berkeley's Omega system; SRI International's PegaSys; Brown University's Pecan; and the University of Southern California's PIP, or Programming-in-Pictures system.

Elevating the software-design process is also the force behind a more conventional programming language. Ada, which promises to upgrade the quality of new software, has witnessed a flurry of activity in the past year. Previously, the language has existed mostly on paper. But as a crop of compilers hits the market, Ada is becoming a force in the engineering world.

This trend should continue as Ada begins its adolescence. "In terms of products, I think you'll see a maturing. Probably most importantly, you begin to see people thinking about the full life-cycle of an Ada program," says Larry Druffel, former head of the DOD's Ada Joint Program Office. Druffel is now in charge of marketing at Rational, which recently introduced one of the first tools aimed at Ada life-cycle support. The Mountain View, Calif., company's R1000 computer-based system is aimed at boosting programmer productivity as well as life-cycle support on large-scale projects such as those in defense contracting.

Ada watchers will also be following developments at Carnegie-Mellon University's new Software Engineering Institute. Observers expect the institute to get clear direction from John

H. Manley, an Air Force veteran who recently took command of the DOD-sponsored institute. The institute will oversee efforts to improve software-engineering techniques for DOD use and ease Ada's move into the software mainstream.

Industry will also look closely at the Software Productivity Consortium [*Electronics,* Sept. 16, 1985, p. 14]. The new group represents 15 aerospace companies, all of which will be adopting Ada. "Clearly, both the Software Engineering Institute and the Software Productivity Consortium are going to be big players in the Ada world," Druffel says.

In home computer software, the trend continues away from entertainment and education toward productivity products—word processing and communications, says Hilda Uribe, senior analyst at Future Computing Inc. Word processing is by far the most popular application, used by 59% of home computer owners, according to the Dallas market researchers.

Computer owners are using business software in the home as well. The survey shows that 39% of home computer users bring work home from the office. In addition, 21% of all personal computer owners run a business from the home.

The availability of software will be critical to the acceptance of new machines from Atari Inc. and and Commodore International Ltd. Volume shipments of Atari's 520 ST are just getting under way; Commodore's Amiga is due to follow. For the 520 ST, a 1-2-3-like spreadsheet from VIP Technologies, Santa Barbara, Calif. is in the works. Digital Research Inc.'s GEM Write and GEM Paint are scheduled for release soon.

Some recent rumblings indicate turbulence for the home computer industry in the coming year. One sign of turmoil was the ouster of Steve Jobs as chairman of Apple Computer Inc. But this may presage a return of the company to its roots. Apple has gone to more than 20 independent software vendors for programs to support a new line of Apple II hardware accessories. An expandable, easy-to-customize Macintosh dubbed Open Mac is said to be on the drawing board.

Meanwhile, Future Computing, regarded as the most optimistic of the market forecasters, is sticking to its guns in suggesting that the potential market is broadening for personal computers sold for home use. But "consumers have to be convinced that a personal computer is a functional appliance that's worth having," warns Uribe. Otherwise, "the only purchasers of computers, peripherals, and software will be people who've already sold themselves." ☐

Reprints of this five-part report will be available at $6 each in November. Send a check or money order to Electronics *Reprints, 1221 Avenue of the Americas, New York, N. Y., 10020. Write for quantity prices.*

STEELE'S GUIDING HAND MADE POSSIBLE COMMON LISP

by Jesse J. Leaf

The silver-covered book looks and feels formidable. Indeed, *Common Lisp* by Guy L. Steele Jr. culminates a historic electronic conference, which resulted in a language that has become the de facto industry standard.

Like most watershed ideas, Common Lisp had colorful origins. In the spring of 1980, three young computer-language experts—Steele, Richard P. Gabriel, and Jon L. White—were driving on a California freeway. They had just left an informal Lisp workshop convened by the Defense Advanced Research Projects Agency to determine the language's status and direction.

Each man represented a different implementation of Lisp. The product of their discussion sounds like something out of Tom Swift: "Gee, why don't we get together on a compromise language?"

Steele, then an assistant professor of computer science at Carnegie-Mellon University, volunteered to coordinate the effort. What he did was oversee a growing electronic network that reached an informal membership of 70 people—all by word of mouth. "Rather than having face-to-face meetings, like most standards committees, we worked almost exclusively by electronic mail over Arpanet."

From Boston, Pittsburgh, Stamford, Conn., Texas, Utah, and California for 2½ years, some 3,000 messages bounced back and forth. From one line to 20 pages, some 1,100 pages of discussion made up the electronic conference.

"It worked so well we didn't feel the need for any face-to-face meetings. In fact, we held two face-to-face meetings, and they didn't work out all that well," says Steele. "Electronic mail gives you time to respond—you don't feel like you have to make an answer that minute or the moment is lost. You can take a half hour or a day or a week to produce a reasoned response."

Fed intellectually by their electronic umbilical cord, the far-flung group completely rethought Lisp. "We looked at many dialects and many features of the dialects. We tried to pick the things that experience showed were good and we also tried to get rid of old ideas that turned out to be not so good—those that were incompatible or not portable."

The result is a compromise language based on MacLisp and ZetaLisp, with accents from InterLisp, Portable Standard Lisp, and others. "People are happy with what happened, and although the language ended up not the way I would have designed it if I had done it myself, I think it is an extremely good compromise among the needs and desires of the entire user community. It is more important that people agree on it than it be perfect."

The Lisp effort has spanned Steele's professional career. After teaching for 2½ years at Carnegie-Mellon, Steele, who was 31 on Oct. 1, wanted to broaden his experience, and began work at Tartan Laboratories Inc., "partly because I wanted to learn about compiler construction under Bill Wulf," chief executive officer of the Pittsburgh company.

GUY L. STEELE JR.

In January, Steele, his wife Barbara—a Lisp programmer and a member of the standards committee—and his two children moved to Cambridge, Mass., where he took on the position of Director of Software Development at Thinking Machines Inc. for the connection-machine project. Steele is using Lisp in his work on parallel algorithms and parallel-programming language.

Steele also plans to revise *Common Lisp,* based on his work with the 466-page volume during the past year and a half. But he will remain impartial. "I see my job as a shepherd. I try hard not to have very strong opinions as to what the language should look like. I have my opinions, but I'll only bring them out after listening to others' positions. My job is to maintain balance to collate everyone's ideas. And to strive for a consensus. After all, I'm a committee chairman."

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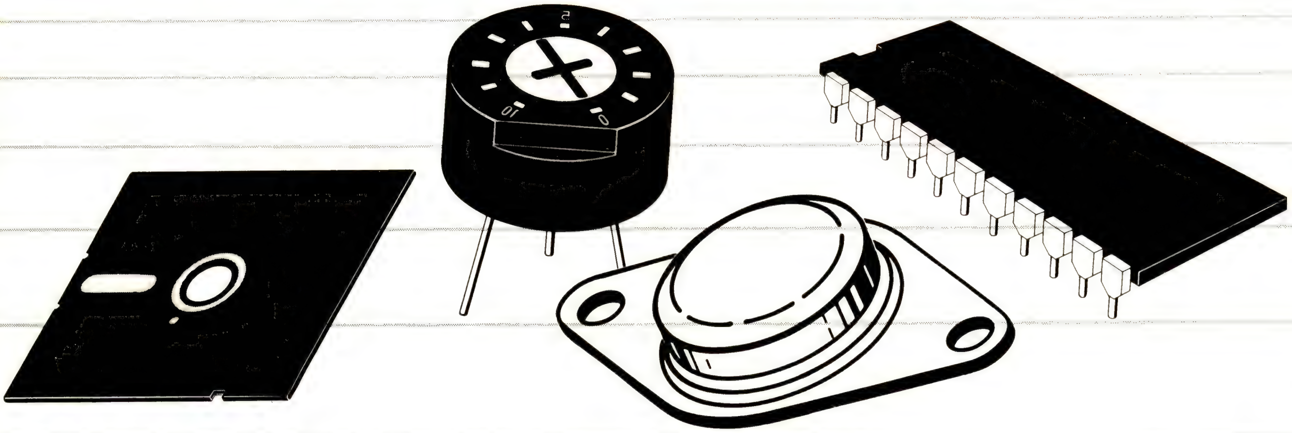

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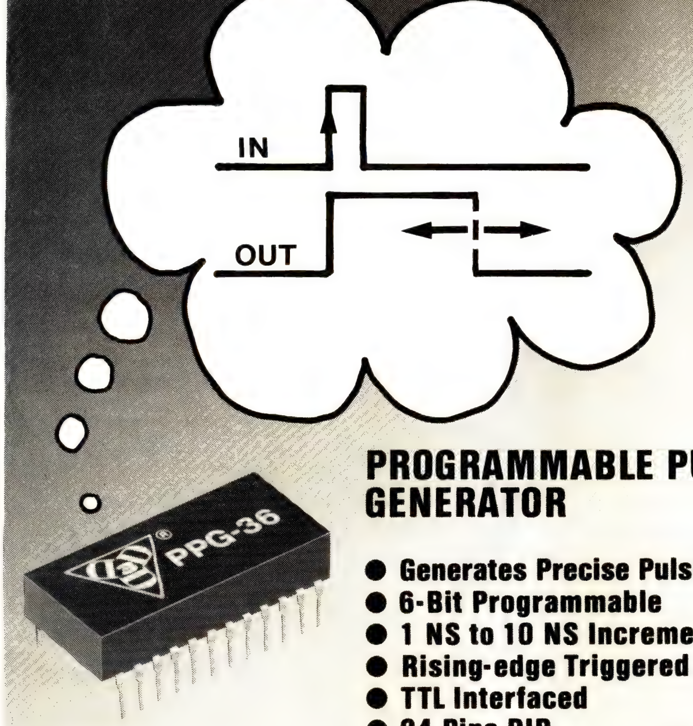

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January

Philips Uses MBE for Lasers
Siemens Readies Commercial ISDN
Japanese Chemical Firm Moves from Soap to Floppies
Italian Firm Seeks Allies to Crack U.S.
Japan Pursues Role in Space
Bellman Switches on Italtel for Expansion
Robots get Smart in Japan
ITT Invests in European Units Crack U.S.

February

Europe's Esprit Finally Sets Sail
LSI Logic Counts on Sandfort to make its Mark in Europe
Upstart Vendor Makes Waves in Japan's Robot Market
NEC Fashions New Fab Process
Olivetti's Viti Directs ET Designs that Marry Bus & Art
German Startup's Success Surprises Europeans
Britons Seek Tolerant Chips
OBI Rains on IBM's Parade
Mega's Friedrich Aims to Cut Asian Lead in Memories

March

British GaAs Chips Go to Market
NEC's CPU Leapfrogs IBM
Hitachi CPU Challenges IBM
France's Lansat Rival Set for Fall Launch
Olivetti Stakes Claim in Video Typewriters
Italian VLSI Chip has the Right Accent
Koreans Try for VCR Replay
Germans Push X-ray Exposure
There's Life in Resistors, German Company Finds
UK Beats a Path for Europe's Race

April

German System Meets New ICAO Standard
West Germans Squabble Over Choice of IFF
Britain Promotes Open Architecture
US Makes Progress in Japan Telecom Talks
Japan's Lead in Optical Disks: It's Part of the System
Daisenberger Guides US Firms through Red Tape
Asia: It's No Longer Just Japan That Threatens US Markets
Malaysia: Top Shipper of Discretes
Indonesia: Domestic Sales are the Lure

May

Thomson's VCR System Clears Up Doubts
ICL Banks on Networks and Japanese Chips
Min Blazes Bright Path for Korea's Gold Star
Asia: The Four Dragons Rush to Play Catch-up Game
Singapore Casts Lot with Software
Philips' Eurom Chip Finally Debuts
Sagging Prices Sting Japanese Producers
British Telecom Spreads Its Wings with Mitel
South Korean IC Maker Seeks World Markets

June

Plessey Switches Off Flash ADC, Saves Power
Sony Campaigns Hard for BMM Camcorders
Japanese Quit on IBM Software, Turn to UNIX
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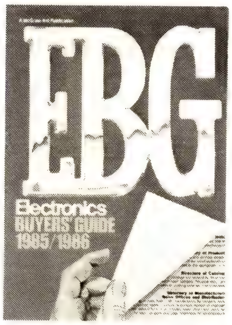

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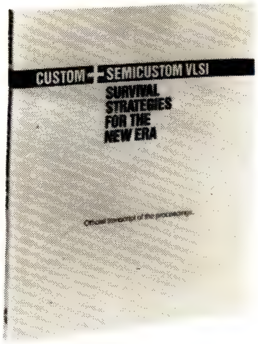

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PRODUCTS NEWSLETTER

INTEL MICROSYSTEM OUTPOWERS VAX-11/780, YET SELLS FOR LESS

Intel Corp.'s new line of Xenix-based multiuser, supermicrocomputer systems sets a new price/performance ratio. The company's systems group in Phoenix claims the high-end version has more than five times the performance of a VAX-11/780, yet it sells for $35,000. The 11/780 typically costs $250,000. Employing four 8-MHz 80286-based CPUs in a master/slave configuration, the high-end 286/310 Apex-4 (for Advanced Processor Extension) system cranks out 5 million instructions/s. The master CPU dispatches tasks to other processors according to a system load-balancing algorithm. The four-processor Apex-4 and three-processor Apex-3 will be available in January, while one- and two-processor models are available now. ☐

LASER SYSTEM BOTH INSPECTS AND REPAIRS SOLDER JOINTS

A computer-controlled infrared-laser system sheds extra light on defective solder joints. After inspection, it will even automatically reflow the bad solder joints of components to the printed-circuit boards. Vanzetti Systems Inc., Stoughton, Mass., is selling the new PDP-11-based Laser/Inspect/Reflow system for about $300,000. The system checks soldered joints by injecting heat to contacts with short pulses from an yttrium-aluminum-garnet laser. Each soldered joint has a unique thermal signature, and a bad joint will cool off slower than a good one. Measurements taken by an IR detector are compared to a data base of known-good signatures. Inspections are done at a rate of 10 per second, and repairs take 0.5 s per joint. ☐

OP AMPS SAID TO OUTPERFORM OTHERS IN SPEED-PRECISION COMBINATION

VTC Inc. is making samples available of the first two units in its new family of operational amplifiers. According to the Bloomington, Minn., company, op amps available from other suppliers can match or outperform its parts in either speed or precision, but none can equal the speed-precision combination of the new line. The VA705, for example, features slew rates of 35 V/μs, a 2-mV maximum offset voltage, a 15-nA offset current, and an output current of ±50 mA. Prices range from $2.57 to $6.20 each. ☐

NEC ENTERS STANDARD-CELL MARKET WITH A 1.5-MICRON CMOS PROCESS

NEC Corp. has entered the merchant standard-cell IC business with a 1.5-μm CMOS technology. Previously the Tokyo company had offered such products in house and to selected customers. With a fanout of three, propagation delay per gate is typically 1.4 ns. The cell library, which consists of over 130 parts, includes one- and two-port static RAM modules with an access time of 20 ns. Delivery takes 10 to 15 weeks after logic simulation. For a 3,000-gate part, the price would be 70% that of a gate array. ☐

FAIRCHILD UNVEILS 5-MIPS 32-BIT CHIP SET

Fairchild Camera & Instrument Corp. is entering the 32-bit CMOS microprocessor market with a three-chip module that offers five times the performance of a Digital Equipment Corp. VAX-11/780. The Clipper module executes instructions in 30 ns, or at a 5-million-instructions/s clip. It will enable microprocessor-based systems to do tasks that were until now only in the preserve of mainframes or superminicomputers: simulation and the design of very large-scale integrated circuits, for example. The Mountain View, Calif., company's module uses the basic elements of a reduced-instruction-set architecture and runs under the Unix operating system. Samples of the $2,451 module will be available in June 1986. ☐

HOW TO TRY OUT A DESIGN STILL IN THE CONCEPT STAGE

CALMA'S SIMULATOR FLUSHES OUT ERRORS BEFORE DESIGNER COMMITS

16 BITS. Using TexSim/B, Calma has simulated a 16-bit 68000.

Computer simulation of chips and boards has one major flaw: designs must be nearly complete before new ideas can get a good spin. General Electric Co.'s Calma subsidiary wants to remedy that with a simulator software package that lets work station users try out designs fully even though much of the design may be still in the conceptual phase.

The package—which is called TexSim/B, for Tegas Extended Simulator, Behavioral—can run comprehensive simulations from any combination of behavioral-, gate-, or transistor-level descriptions. "This can be of help because many times you don't exactly know how you are going to implement a particular design. However, you might know something about how parts of it are expected to behave," says David Niehaus, design products marketing manager at the Austin, Texas, company. "You can save a lot of time flushing out errors early before committing to a technology for implementation."

Calma believes TexSim/B is the first package that allows full simulation of designs under mixed modes of behavioral, gate, and transistor descriptions. A number of behavioral packages on the market will not operate fully with some devices described as gates and some as transistors. Niehaus suggests that the conversion process between behavioral models and more detailed design implementations opens up the possibility of errors and inadvertent changes in the models. The need for mixed-level design simulation is on the rise as engineers attempt to tackle more complex products on work stations, he adds.

TexSim/B is an expanded version of Calma's TexSim simulation package, which is standard on the company's TegaStations. The Calma work stations, ranging from $24,500 to $90,000 each, are based on hardware from Apollo Computer Inc. TexSim/B, an option for the TegaStations, sells for $20,000. Calma plans to begin production shipments of the simulation package within a month. The simulation software will be demonstrated at the upcoming Automated Design and Engineering for Electronics conference, to be held Oct. 15-17 in Boston.

The behavioral-simulator software can verify the design of very large-scale integrated circuits, semicustom chips, and pc boards. The description of functional blocks is written from high-level system specifications using the Tegas Design Language/Behavioral. Verification of behavioral models can be speeded up with a structural debugger.

TexSim/B contains some 76 primitives, such as gate and functional descriptions of logical devices. These represent a wide range of simple Boolean gates, such as flip-flops, to more complex arithmetic logic units. Calma's design-automation software engineers have modeled an entire 16-bit 68000 microprocessor to run in the behavioral simulation. After testing is complete, the behavioral model of the 16-bit processor will be placed into the simulation library and available to customers by early 1986.

Using the 68000 behavioral model, for example, pc-board makers could run more detailed gate-level simulations of board designs before committing to a specific semiconductor technology. Calma plans to create other microprocessor models, including one for the 32-bit 68020.

"What makes TexSim/B so powerful is its capability to handle the mixed-level modes," says Niehaus. "Some designers like to describe circuits behaviorally to document the entire system and flesh it out architecturally. Then designers can selectively take pieces and decompose descriptions down to the gate or transistor levels, allowing verification of the precise timing that is required." *–J. Robert Lineback*

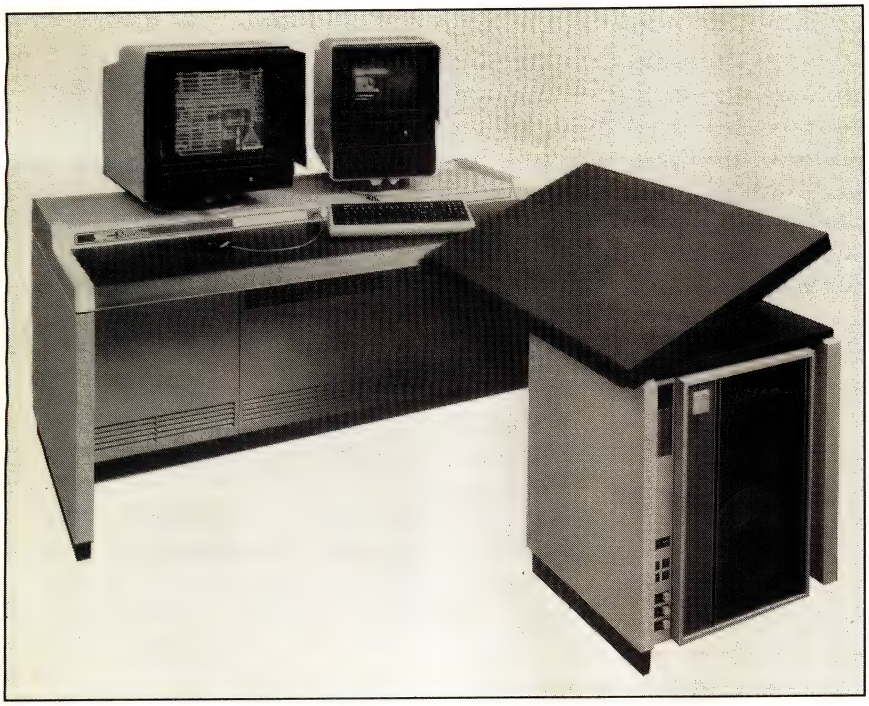
Calma Co., 12096 Park 35 Circle, Austin, Texas 78753. Phone (512) 339-0779. [Circle reader service number 338]

EASY-TO-USE SOFTWARE FOR CAE RUNS ON IBM PC

The market for low-end computer-aided-engineering equipment is crowded with products that claim superlative results and ease of use for a minimal price. Ruled by price/performance ratios and the demand for compatibility with existing systems, the market is a fickle one and competition is fierce.

But Scientific Calculations is challenging that fickle spirit with Scidesign, a $7,000 CAE program for use on IBM Corp. Personal Computer/XTs and ATs. Scidesign, which will be unveiled at next week's Automated Design and Engineering for Electronics conference in Boston, can also be used with the company's higher-end VAX-based CAE products. This gives the designer capabilities not found on other PC-based systems.

Scidesign is a desktop system intended for electronics design engineers who might use their IBM PCs for other engineering and business applications. It requires minimal hardware adjustments and offers a simple menu-driven interface. To run the program, the PC needs a graphics card, a math coprocessor chip, and a mouse and interface.



VERSATILE. Scidesign runs on IBM PCs but links with Scientific's VAX-based software.

"We paid a lot of attention to the user interface," says David Magellan, assistant product manager for Scidesign. So for users who cannot commit to memory the complex set of commands most systems rely on, Scientific Calculations developed an expandable menu format, with consistent syntax throughout. This allows the novice user to avoid the reeducation process he might encounter if he had to do the work on a more sophisticated work station.

COMPATIBLE. Scidesign was developed for use with Scientific Calculations' Scicards and Schemactive programs. Scicards is a high-level design tool for a complete 32-bit multiuser system such as Digital Equipment Corp.'s VAX units. The company bills it as a total design solution for printed-circuit boards that employ hybrid and surface-mounting technology. Schemactive is used for creating complex schematic diagrams. It can generate schematic and logic drawings up to 100 pages in length.

Scidesign and the higher-end programs all share the same unified database, providing complete synchronization between the IBM PC-based system and the dedicated minicomputer used for running the high-end software. Integration with the Scicards program allows the user to upload the engineering design to the VAX, and receive annotation following gate assignments and layout. Without that synchronization, says Magellan, refinements that are made using Scicards to a design generated on Scidesign cannot be transmitted to the PC. This means that any changes have to be made using time-consuming manual methods.

"This ability to maintain proper synchronization is unique in regard to Scicards," Magellan says, adding that no other vendor has a PC-based product that could fully share information with the Scicards system. Scicards takes information generated by Scidesign and compares it to three of its six libraries for shapes, parts, and functions.

"With Scidesign you are doing two things," according to David Jarvie, assistant product manager for Scicards. "You are creating the symbols for a schematic design, and then you are creating the geometry between the symbols. That information is checked against those three libraries to generate the net list for the Scicards algorithms."

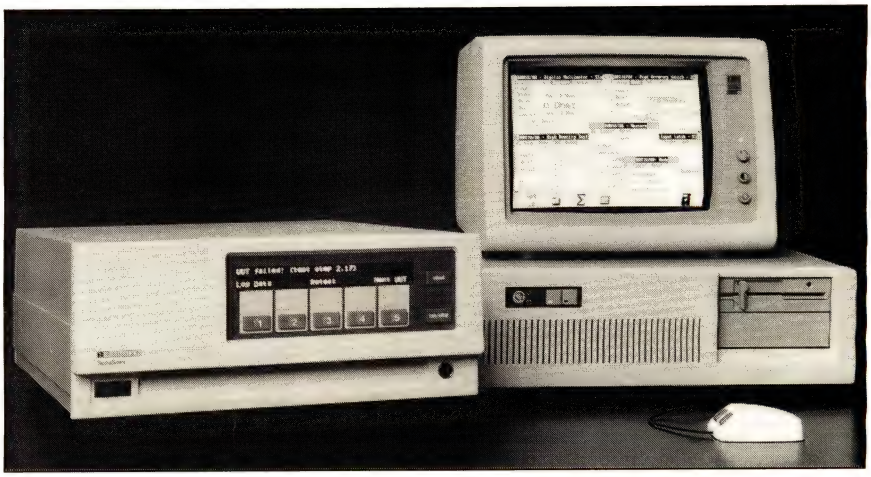
Because Scidesign has its own dedicated graphical symbol editor, the user can manipulate primitives and other graphic information, Magellan says. The program generates schematics by means of two-segment routers, and it offers a choice between standard and user-defined sheet sizes. Users can add, delete, or move both symbols and interconnection lines, and the program can rotate and scale symbols as well. Scidesign has a symbol library of more than 500 TTL, ECL, and CMOS symbols. It is available now. *–Tobias Naegele*

Scientific Calculations Inc., 7635 Main St.,
Fishers, N. Y. 14453.
Phone (716) 385-6790 [Circle 339]

FINAL-TEST SYSTEM SUITS JUST-IN-TIME ASSEMBLY

The rush to adopt such manufacturing concepts as just-in-time manufacturing, total quality control, and computer-integrated manufacturing is placing new demands on final-assembly testing in the factory. Summation's answer is the SigmaSeries, comprising a 68000-based integrated TestStation, which accommodates plug-in instrument modules; proprietary TestWindows program development and interface software; and an IBM Personal Computer AT-compatible computer.

"The just-in-time concept says that you can produce one product just as cheaply as you can 1,000 things," according to Jim Bloomer, president of Summation. This means that test sys-



FINAL TEST. Summation's modular system aims to end traditional rack-and-stack test gear.

tems must be fast and reconfigurable. The SigmaSeries is a fully integrated general-purpose automated system for final-testing applications that meets these demands.

Traditional production testing, which has been served by controller-based rack-and-stack instrument clusters, has fallen short. "Rack-and-stack test systems are complicated to integrate, difficult to program, weren't meant to run together in networks, and require skilled operators," Bloomer says. They are also expensive, typically costing $100,000 for customized gear. Summation tackles the problem with a low-cost modular system that is easy to reconfigure for each new testing application and that collects and analyzes test data.

Only 7 in. high, the test station contains analog and VMEbuses that supply a highly integrated stimulus and measurement environment. The plug-in modules, which can be synchronized to within 50 ns, simultaneously share signals and automatically trigger off each other. Special programmable switch modules route stimulus and measurement signals to the unit under test as directed by the user's program. With only seven keys and a vacuum fluorescent display for prompting the operator, the TestStation is easy to use.

Both analog and digital stimulus and measurement functions are available. When unveiled at Wescon in San Francisco next month, the TestStation system will have 11 modules, including a breadboard unit that will let customers build custom modules such as filters. Others include a waveform recorder, function generator, and multimeter.

The system's analog capability is up to 10 MHz, with switching up to 200 MHz. Digital inputs and outputs have up to 50-ns resolution and time-interval measurement to zero. Up to 1,320 low-voltage, 440 high-voltage, and 132 high-frequency inputs can be switched.

Programs, which the user writes in an extended Basic language called TestBasic, are controlled in a proprietary environment that uses windows and icons similar to the Apple Macintosh's. TestBasic includes powerful debugging utilities, structured programming tools, and local variables for library functions.

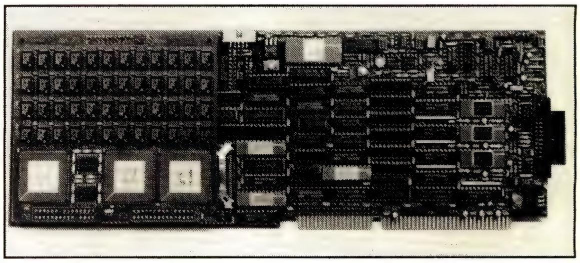
Bloomer says that because most engineers are already familiar with Basic, writing test programs with TestBasic will take about one fifth the time it does to create programs for rack-and-stack instrument clusters. The software incorporates the Import/Export feature, which automatically converts the user's menu settings to IEEE commands.

In mid-1986, Summation aims to tackle the broader issues of computer-integrated manufacturing with an enhancement called SigmaNet that will link numerous SigmaSystems and computers. Without computer, SigmaSystem sells for under $20,000. Delivery takes 12 weeks after ordering. *–Steve Zollo*

Summation Inc., 18072 142nd Ave. N. E.,
Woodinville, Wash. 98072.
Phone (206) 486-0991 [Circle 339]

IMAGE PROCESSING BOARD COSTS ONLY $4,000

Real-time image-processing systems are about to grow in performance and drop in price. At this week's Electronic Imaging Show in Boston, Imaging Technology will announce its Series 100 single-board image processing subsystems, which boast high resolution and offer capabilities that until now were available only in more expensive multiple-board sets.



MIGHTY. Imaging Technology's single board packs the image-processing capabilities usually found on multiple-board sets.

The boards, which average $4,000 each, come in versions for use in VMEbus-, Multibus-, and Q-bus-based systems, and in the IBM Corp. Personal Computer AT. An earlier product from Imaging, the IP512 three-board subsystem, sells for $10,000.

The boards feature a resolution of 512 by 512 pixels by 12 bits; similar products offer frame memories with 8-bit-deep pixels. As many as 256 gray levels are available. Sixteen lookup tables per output channel can provide up to 4,096 shades of gray for pseudocolor display. In addition, the boards have feedback circuitry for the input lookup tables that allows software to modify incoming and stored images in real time.

The boards' 12-bit-deep pixels provide several different modes of operation. In one mode, images with 256 gray levels can be stored using eight of the bit planes and graphic overlays can be displayed using the remaining four.

To consolidate the multiboard subsystem onto one board, the company used gate-array and surface-mounting technologies. Each 1-in.^{2} custom gate-array chip replaces from 50 to 150 conventional TTL chips. Moreover, the use of surface-mounting technology further increases chip density and allows Imaging to implement a lot of basic algorithms in hardware.

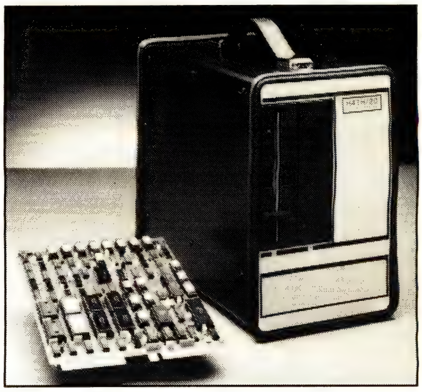
"The real-time capabilities of the hardware eliminate the need to develop software for performing on the host fundamental image-processing algorithms such as image subtraction," says Robert Birenbaum, product marketing manager for Imaging Technology. "The processing element—the feedback/input lookup table—is fully programmable, so that multiple operations can be performed on the pixel data during a single frame time."

The Series 100 accepts analog video inputs from standard RS-170 or RS-330 sources. The boards sell for $3,995 for the monochrome version and for $4,495 for pseudocolor model. The PC AT version is available now, with the other versions scheduled for delivery in the fourth quarter. *–Debra Michals*

Imaging Technology Inc., 600 West Cummings Park, Woburn, Mass. 01801.
Phone (617) 938-8444 [Circle 341]

SINGLE-BOARD ENGINE SUPPORTS 7 USERS

The Forth multiuser, multitasking programming environment—popular for process control and instrumentation—has been enhanced by the H4TH/x Forth engine, which supports up to seven users. The series includes the H4TH/01 single-board computer for



original-equipment manufacturers and the desktop H4TH/20 system for program development and vertical-market applications. On these systems, the Forth language has been microcoded, as has a major part of the operating system, and all high-level functions have been written in Forth.

As an example of the Forth engine's performance, it executes the sieve of Eratosthenes benchmark in 9 s. The single-board computer, priced at $2,000, includes a microprogrammed bit-slice processor with 1-K by 32 bits of microprogram memory and 48-K bytes of local RAM. The desktop H4TH/20 is based on the single-board computer, plus a backplane, floppy-disk and hard-disk storage, up to 2 megabytes of RAM, 18 serial I/O ports, a Shugart Associates System Interface bus, and other features. It sells for $11,400.

Hartronix Inc., 1201 N. Stadem Dr., Tempe, Ariz. 85381.
Phone (602) 966-7215 [Circle 359]

TWO 32-BIT CHIPS RUN WORK STATION

The HostStation line has been topped off with the 550 desktop work station, which uses two 32-bit processors for computation and graphics processing. Its 19-in. monochrome display offers a resolution of 1,056 by 864 pixels. Standard features include floating-point math processing and memory management; 1 megabyte of main memory, expandable to 2 megabytes; 41 megabytes of internal hard-disk storage, expandable to over 370 megabytes; and integral Ethernet and Cheapernet interfaces.

The Umax operating system is a multitasking operating system that is Unix-compatible. Initial software includes C, Fortran, and Pascal compilers as well as graphics support. The HostStation 550 is compatible with VT100 and several other terminal protocols and offers three RS-232-C ports. Options include additional hard- and floppy-disk data-storage units, a 60-megabyte streaming-tape drive, and a mouse. Priced at $14,000, the HostStation 550 carries quantity discounts for original-equipment manufacturers. It is available this month.

Encore Computer Corp., 257 Cedar Hill St., Marlborough, Mass. 01752.
Phone (617) 460-0500 [Circle 358]

CHIP RESISTORS RETAIN ID MARKINGS

The CR21 and CR32 chip resistors have face-up markings that maximize heat dissipation. The markings also let them be identified on the board even after dual-wave-flow or vapor-phase-reflow soldering. The resistors have power ratings of 0.1 W to 0.25 W, respectively, and feature nickel barrier terminations.

The devices come in resistance values from 10 Ω to 2.2 MΩ at tolerances of 2% and 5% and with a temperature coefficient of 300 parts per million. Resistors are also available with values ranging from 100 Ω to 1 MΩ at tolerances of 1% with a 100-ppm temperature coefficient.

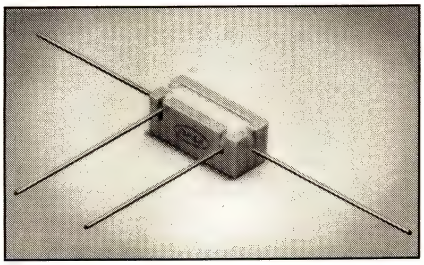
Available from stock, the resistors with a 5% tolerance cost less than 2¢ per chip in quantities of 10,000. They are available in bulk, on 8-mm tape reels, or in magazines.

Kyocera International Inc., Electronic Components Group, 11425 Sorrento Valley Rd., San Diego, Calif. 92138.
Phone (619) 454-1800 [Circle 381]

RESISTOR HAS 4 LEADS FOR CURRENT SENSING

Dale Electronics' CPSL commercial power wirewound resistor provides four leads for use in circuits that require current sensing, including current monitors, feedback control loops, overload sensors, and motor controls. Available in 3-, 5-, 7-, 10-, and 15-W sizes, the resistors have a high power-to-size ratio.

For example, the CPSL-5 dissipates 5 W from a body size of ⅞ in. long by ⅜ in. high by 11/32 in. wide. The standard tolerance of the resistor is ±5%, and resistors ranging from 0.01 Ω to 0.10 Ω are available.



In lots of 1,000 pieces, a 5-W 0.01-Ω resistor sells for 52¢ each. Parts are available now.

Dale Electronics Inc., 2064 12th Ave., Columbus, Neb. 68601.
Phone (402) 564-3131 [Circle 380]

SMART POWER FETS HANDLE 12 AND 15 V

The Smartpower family of circuits for overvoltage and overtemperature protection now includes models that cover the 12- and 15-V power buses. The product family now includes seven parts, including 7.5-, 15-, and 35-A devices for 5-, 12-, and 15-V circuits.

The devices are part of the Smartpower II process, which combines CMOS logic with a vertical TMOS power device. They are intended to protect voltage-sensitive systems from excessive voltage transients as well as from extreme temperatures.

The 7.5-A devices, the MPC2004, the 2011, and the 2014, will sell for under $1.00 in lots of 10,000 pieces. Delivery is from stock but may take up to 12 weeks after ordering.

Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Ariz. 85036.
Phone (601) 244-4911 [Circle 382]

IBM PC-BASED SYSTEM ANALYZES MOTION

The DM-1000 system for motion-data acquisition samples and updates information at a rate in excess of 20 kHz per axis. It uses up to six resolvers to sense position and an IBM Corp. Personal Computer to record and display data. The DM-1000 consists of an interface card, which plugs into a long expansion slot of the PC, PC/XT, PC AT, or compatible, and software drivers that interface to Basic or such high-level languages as C and Compiled Basic.

The motion system is designed for machine automation, robotics, and two- and three-dimensional position and velocity monitoring for computer-aided design. The data from all axes can be frozen simultaneously before being read to provide true real-time data. This feature allows the user to perform multiaxis contouring and true differential position analysis and profiling, according to the company.

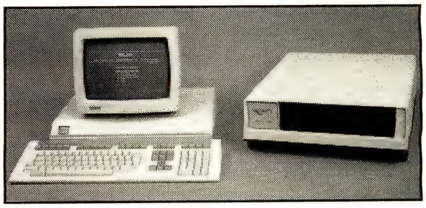
The DM-1000 received all of its power from the host computer and is electrically isolated from external machine wiring. Available six weeks after ordering, a six-axis system sells for $1,395.

Data Motion Corp., 1785 Cortland Ct., Addison, Ill. 60101.
Phone (312) 495-2158 [Circle 378]

DATA SYSTEM BUILDS CONTROLLERS

Integrated Systems' MAX 100 high-performance real-time control implementation processor and data-acquisition system implements nonlinear multirate controllers that users create with the company's Matrix control-design package.

The direct implementation allows control engineers to quickly evaluate the performance of their designs on real hardware, the company says. The MAX



100 can be connected to a host computer for transferring designs and data, or it can be used as a stand-alone system in the field.

Data gathered with the MAX 100 can be brought back to the host for analysis with Matrix. Once in Matrix, the data can be manipulated, filtered, and analyzed in the time or frequency domains.

The MAX 100 can run a 12th-order, four-input, four-output controller at rates up to 100 Hz concurrently with a 12-parameter, 90-state identification algorithm at 20 Hz. Priced at $40,000, MAX 100 is available in 30 days.

Integrated Systems Inc., 101 University Ave., Palo Alto, Calif. 94301.
Phone (415) 853-8400 [Circle 379]

GATE ARRAY IS FIELD PROGRAMMABLE

The 82S151 field-programmable gate array permits users to generate custom patterns using standard programming equipment. The model 82S151, which is the final addition to Signetics Corp.'s Applications Specific Products Division's family of field-programmable products, is a 20-pin single-level logic element consisting of 12 NAND gates with fusible-link connections for programming I/O polarity, I/O direction, and output-enable control.

All gates are linked to the 6 inputs and the 12 bidirectional lines, so virtually any combination of inputs and outputs can be configured. The part is specified at a propagation delay of just 15 ns with a typical power dissipation of only 0.65 W.

In lots of 100 pieces, the commercial version is priced at $2.08 each and is available now.

Signetics Corp., 811 E. Arques Ave., P. O. Box 409, Sunnyvale, Calif. 94086. Phone (408) 739-7700 [Circle 376]

ARRAY CAN FIGURE SUM-OF-PRODUCT

Thanks to its AND-OR-Invert architecture, Silicon Systems' CMOS mask-programmable logic array lets the user implement custom sum-of-product logic equations. The TTL-compatible 82C100/101 incorporates 16 inputs and eight outputs to yield a total of 48 available product terms.

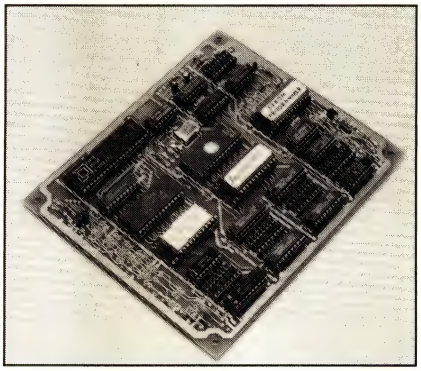
Each product term is the logical AND of up to 16 of the inputs in true or complement form. All these product terms can be linked with OR connections to create a desired output function. The output can then be programmed as active high or low.

The device has a 50-ns typical address-access time and is housed in a 28-pin DIP. Priced at $5.50 each in lots of 5,000 pieces, the array is available now.

Silicon Systems Inc., 14351 Myford Rd., Tustin, Calif. 92680.
Phone (714) 731-7110 [Circle 377]

CONTROL CARD HOLDS FORTH IN EPROM

The model SBC88, a single-board industrial development and control system, is supported in Basic or, for high-speed applications, in Forth. Programs are written into the onboard RAM. Then a proprietary algorithm programs up to 24-K of source code into the EPROM.



Once stored, these programs automatically execute whenever power is supplied to the system. Built-in commands download programs from a personal computer or accept hexadecimal files as produced on an Intel Corp. or Digital Research Inc. assembler.

The subsystem consists of two 8-bit input and two 8-bit output ports, seven individually addressable inputs, and seven high-current—500 mA, 50 V—outputs. An 8-bit analog-to-digital converter creates eight channels of analog input. Analog output is implemented through software as well.

For 1,000 units, the SBC88 sells for $99 each; delivery is from stock.

Vesta Technology Inc., 7100 W. 44th Ave., Suite 101, Wheatridge, Colo. 80033.
Phone (303) 422-8088 [Circle 362]

CHASSIS ADDS USERS TO THE IBM PC AT

An expansion system that uses Intel Corp.'s 80286 microprocessor and runs under PC-DOS or MS-DOS, turns the IBM Corp. PC AT and compatibles into a multiuser system supporting up to four users. The Multi-AT/4 uses an eight-slot expansion chassis to connect the work stations. It also provides room for up to 640-K bytes of memory.

Multi-DOS software enhances the computer's performance, thanks to new system calls that shorten response time. Multi-DOS also lets each work station run the same or different programs concurrently and will run color and graphics as an option. Other options include file-locking and a print spooler.

Available now, Multi-AT/4 costs $1,695 for the basic configuration of the expansion chassis, Multi-DOS, and hookup for a second work station.

Anex Technology Inc., 151 N. Rte. 9W, Congers, N. Y. 10920.
Phone (914) 268-2400 Circle 364]

BUBBLE-MEMORY CARD CARRIES CONTROLLER

For industrial original-equipment manufacturers, the iSBC 264 magnetic bubble-memory board provides up to 2 megabytes of nonvolatile mass data storage that will withstand temperatures from 0°C to 60°C.

Since the iSBX 264 board contains an intelligent controller, no extra controller board is necessary for high-throughput operations.

The iSBX board uses the 7114 bubble memory in combinations of one, two, or four cells providing storage capacity of 512-K bytes, 1 megabyte, or 2 megabytes, respectively. The models cost $1,400, $2,100, or $3,600, respectively, in quantities of 100 and are available now.

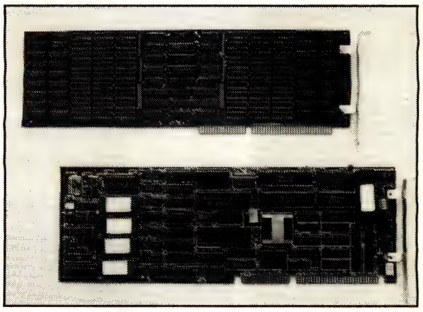
Intel Corp., Literature Dept. W-240, 3065 Bowers Ave., Santa Clara, Calif. 95051
[Circle 365]

BOARDS BUILD PC AT SYSTEM

Three boards offer original-equipment manufacturers a flexible, bus-structured approach to configuring a system compatible with the IBM Corp. PC AT. The Qc1032 processor board is based on the 80286 microprocessor.

The Qc1033 bus-connector panel comes with eight slots. Memory for the system is provided by the Qc1034 memory card, which is $395 for the basic 512-K byte version and can be expanded to 2.5 megabytes. The Qc1032 processor board costs $995, the Qc1033 bus-connector panel is $125, and the Qc1034 sells for $395. All three are available now.

Quam Corp., 2817 Anthony Lane S., Minneapolis, Minn. 55418.
Phone (612) 788-1099 [Circle 363]



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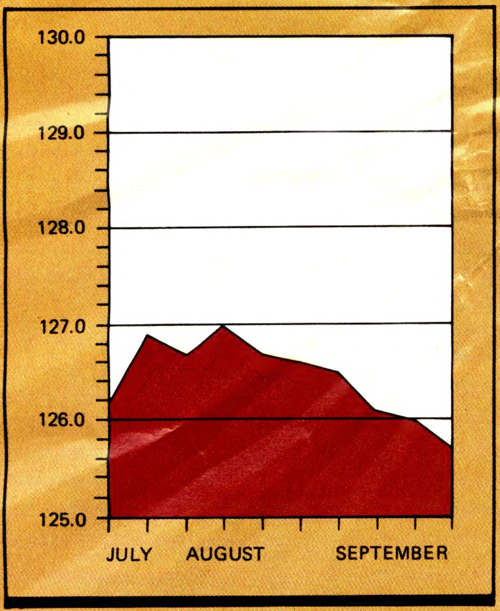
ELECTRONICS INDEX



THIS WEEK = 125.7
LAST WEEK = 126.0
YEAR AGO = 130.8
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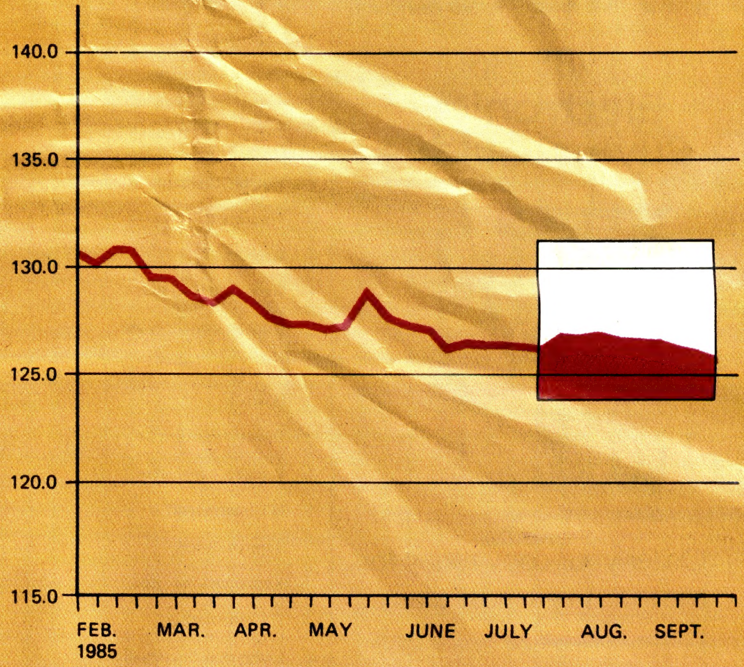

The *Electronics* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U. S. ELECTRONICS IMPORTS & EXPORTS ($ MILLIONS)

	IMPORTS			EXPORTS		
	July 1985	**June 1985**	**July 1984**	**July 1985**	**June 1985**	**July 1984**
Accounting, computing, and data-processing machines	337.949	269.256	375.109	512.356	623.101	589.682
Calculators	39.910	40.132	70.552	7.147	6.156	7.124
Parts for data-processing machines and office calculators	310.903	358.962	451.663	401.183	599.545	565.919
Telecommunications, sound-recording, and sound-reproducing equipment	1,371.490	1,497.511	1,696.795	348.484	346.595	373.902
Electronic or electric instruments	143.104	149.080	149.542	521.459	568.997	540.205
Printed-circuit boards	22.696	24.639	30.499	22.651	25.035	22.511
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	426.861	550.792	915.897	346.901	402.142	522.689
Fixed and variable resistors	18.331	20.716	38.100	11.549	13.101	15.316

The most recent plunge in exports of U. S.-made electronics equipment drove the *Electronics* Index down 0.2% to its lowest level in 16 months. Though imports of electronics equipment in July dipped 8.2%, this was little consolation to U. S. manufacturers who saw foreign markets for their equipment shrink nearly 16%. Worse yet, the U. S. electronics trade deficit increased 53% in July, to $500 million. Nonetheless, the U. S. electronics industry can take heart that some improvement in industry export performance has occurred in the past year. The July 1984 U. S. electronics trade deficit stood at over $1 billion.

U. S. computer makers *were* major casualties of July's trade debacle. Exports for this segment of the industry crashed 18%, while imports of computers and other office equipment surged 26%. Reflecting poor demand, both imports and exports of semiconductors were off in the month.

With interest rates firming slightly, domestic equipment makers can only hope that the U. S.'s major trade partners will continue their concerted effort to drive down the value of the dollar. Though it's too early for the dollar's recent drop to be felt in product prices, the dollar's decline, if it continues, will give added impetus to future U. S. exports.

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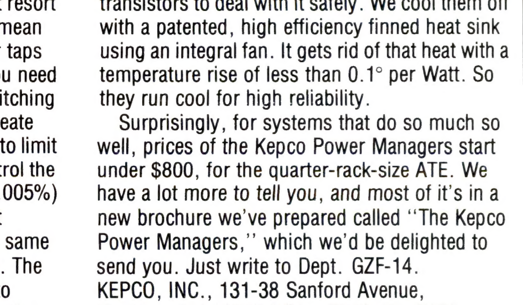

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